ENERGY-OPTIMIZED DESIGN TECHNIQUES FOR WIRELESS COMMUNICATION AND UBIQUITOUS SENSING NODES

A Thesis
Presented to
The Academic Faculty

by

Stephen T. Kim

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2012

ENERGY-OPTIMIZED DESIGN TECHNIQUES FOR WIRELESS COMMUNICATION AND UBIQUITOUS SENSING NODES

Approved by:

Dr. Emmanouil M. Tentzeris, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Jongman Kim
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Shyh-Chiang Shen
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Sung Ha Kang
School of Mathmatics
Georgia Institute of Technology

Dr. Chang-Ho Lee
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: November 29, 2011

ACKNOWLEDGEMENTS

First, I would like to acknowledge the enthusiastic supervision of my research advisor, Professor Emmanouil M. Tentzeris. He has been a source of inspiration and motivation for my research. Without his guidance and support, this research would not be completed.

I am also grateful to my committee members, Professor Shyh-Chiang Shen, Professor Chang-Ho Lee, Professor Jongman Kim, and Professor Sung Ha Kang for for their time in reviewing my thesis.

I would like to specially thank Dr. Joy Laksar and Dr. Kyutae Lim for their dedicated supports, insightful comments and guidance.

I am greatly indebted my colleague members in Microwave Applications Group for their assistance and helpful discussions. I owe special thanks to the cognitive radio team members: Dr. Jongmin Park, Dr. Taejoong Song, Dr. Kwan-woo Kim, Dr. Sanghyun Woo, Dr. Joonhoi Hur, Dr. Jaehyuk Choi, Dr. Sang Min Lee, Dr. Seungil Yoon, Michael Lee, and Dr. Sungho Beck. I also owe special thanks to the senior engineers in Samsung Design Center for their numerous technical discussions.

I am deeply grateful to my wife, Hyun Kyung for her love and encouragement. She has given me the energy and love to stay positive and happy throughout my degree. I also thank my son, Andrew Jungwoo as he is one of the greatest gifts in my family. Also, I owe special thanks to my parents, Soonkee Kim and Soonkyu Park. Throughout my life, they have been the source of endless encouragement. Finally, for all of my family member, this work could not have been completed without their dedicated support, trust and love.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The objective of the proposed research is to analyze and develop energy optimized design techniques that can improve the operating efficiency for a wireless sensor device. To enhance the operating efficiency, all active functional blocks in a system should focus on energy conservation while achieving the required tasks. In addition, variations in the operating condition should be properly observed and compensated. Otherwise, a wireless sensor device would consume unnecessary energy for a given task or too little energy to meet the requirements.

In this research, design strategies and some new circuit topologies are discussed in terms of ultra-low energy constraints. In particular, the signal processing unit, the memory unit, and the power unit in a conventional wireless sensor device will be main focus. As an example of the signal processing unit, a subthreshold current mode computation system has been designed and tested to prove the low power consumption feature of analog signal processing. For the memory unit, conventional SRAM cells are compared to a new fully-gated 10T-SRAM cell. For the power unit, a semi-active high-efficient CMOS rectifier with a reverse leakage control has been developed. It employs a cross-coupled NMOS pair and two leakage control comparators to reduce reverse charge leakage currents. In addition, the adaptive body bias control technique is utilized to improve the reliability of the rectifier.

In addition, a novel link-variation sensing technique is proposed. The proposed technique can evaluate operational disturbances such as component mismatches and displacement variations so that the performance of a wireless sensor device in the actual environment can be close to the optimum without wasting an excessive amount of energy.

CHAPTER I

INTRODUCTION

Advanced complimentary-metal-oxide-semiconductor (CMOS) technology has enabled to integrate multiple functions in a single-chip device that can still maintain reasonably low-power as well as low-cost. While the increased number of functions per integrated chip (IC) from the advanced fabrication technology has been one of the main benefits for high performance electronic instruments, the low-power consumption per a given amount of functions induced from the advanced technology introduced the concept of ubiquitous sensing and wireless communication with a micro-scale sensor device.

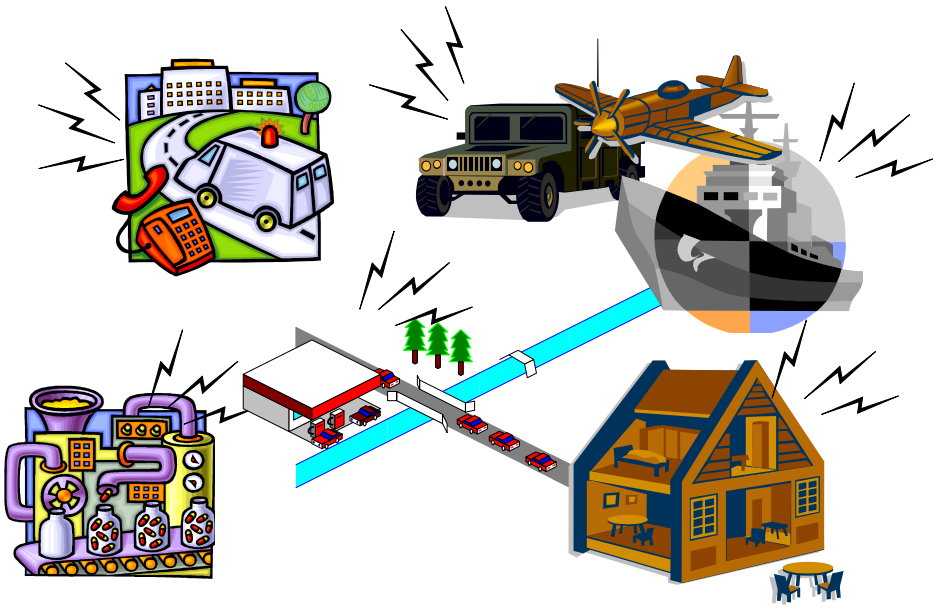


Figure 1: Ubiquitous sensing and wireless communication in military, commercial, and medical fields.

The ubiquitous sensing and wireless communication operation is physically realized by micro-scale sensor nodes. They can monitor and interact with surrounding

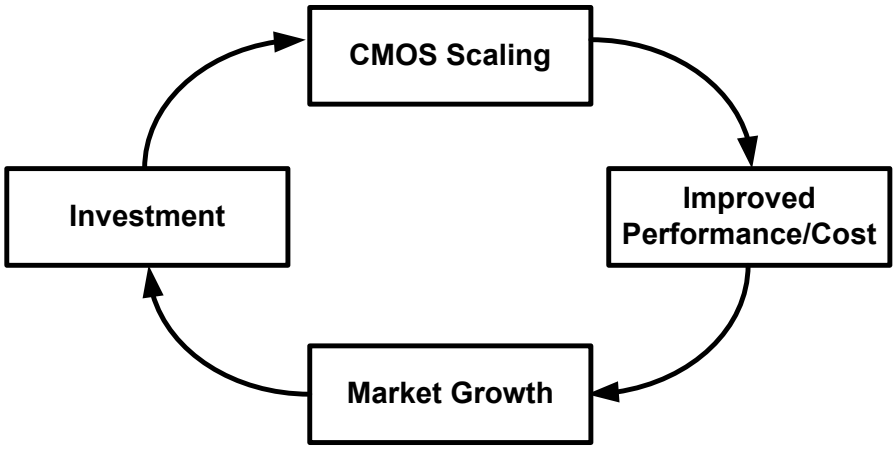


Figure 2: The virtuous circle of the semiconductor industry [4].

physical phenomena, provide *in-situ* signal processing and storing preliminary data, and communicate with other sensors and base units. By doing so, the micro-scale sensor nodes can play vital roles in military, commercial, and medical fields as shown in Figure 1 [2][8].

1.1 Technology Trends

The ever-growing demands for high performance ICs expedited the semiconductor market expansion, and the consequent market growth provided a strong motivation for the CMOS scaling. With the market-driven aggressive CMOS scaling, one can obtain improved performance-to-cost ratio, which completes the virtuous investment cycle for the CMOS industry as shown in Figure 2 [4]. Since the CMOS-based technology proved to be one of the most effective solutions to multi-functional electronic products, and the virtuous circle will continue to improve implementation efficiency, it is natural for any futuristic devices to heavily rely on the CMOS technology.

According to Gene's law [13] as shown in Figure 3, the amount of power consumption to realize a signal processing task decreases as the technology advances. If Gene's law is combined with rapidly growing signal processing demands, one can estimate that the overall estimated power consumption for digital signal processing tasks would

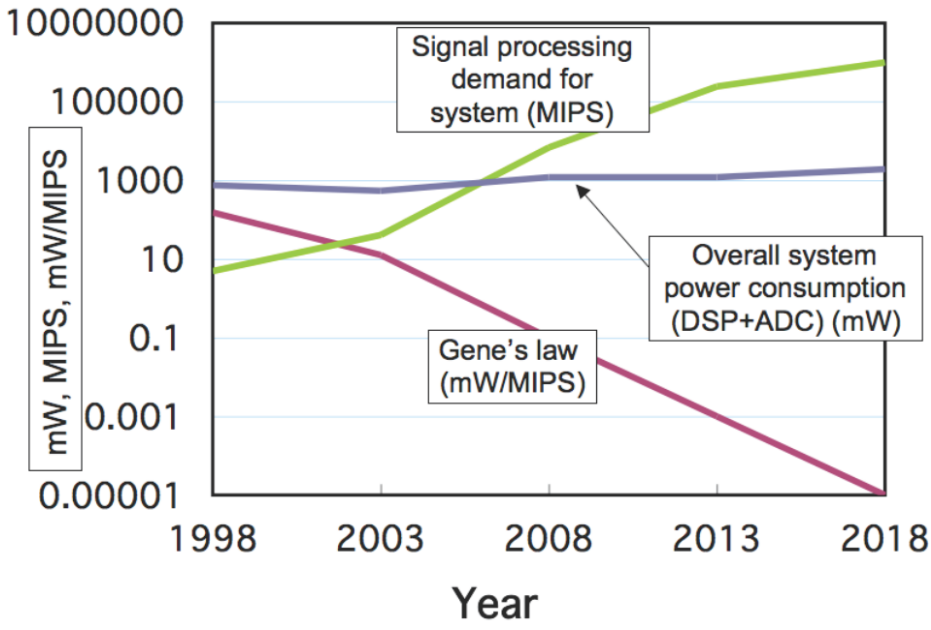


Figure 3: Roadmaps for Gene's law, signal processing demands, and total system power consumption [26].

remain constant. The road maps shown in Figure 3 imply that the advanced CMOS technology would essentially increase the operating efficiency of complex digital signal processing circuits.

However, as every electronic system should ultimately interact with the analog world, the performance improvement in the digital content on an IC by itself cannot satisfy the growing demands for higher added-value products; smarts phones are able to not only perform complex digital signal processing tasks but also provide high-speed wireless data connectivity, touch screen interface, and satisfactory battery management. Analog circuit blocks are required for the analog interface: power management blocks and high frequency RF blocks for wireless communication functions. In addition, mixed-signal blocks are required for frequency synthesis and analog-to-digital conversion. Unfortunately, it is natural for the fabrication technology to lean towards *digital* because, in general, about 90% of the overall functional blocks in a IC is dedicated for digitial circuits. Therefore, the performance of the analog and mixed-signal circuitry does not improve as much as that of the digital circuitry does

from the CMOS scaling. To alleviate this issue, the non-digital functions often have to be realized using separate fabrication technologies. For example, in mobile applications, power management blocks require high voltage tolerance so that they can handle external battery voltages, and they are usually implemented with long channel processes; the average operational Lithium-Ion battery voltage is between 3 to 4 volts, whereas nominal supply voltages of deep submicron transistors are usually below 1 volt.

Consumer demands has driven the modern CMOS technology to be equipped with complex signal processing capability. With the strong processing power, a number of efforts are made to improve the performance of the non-digital content on CMOS technology so that a wide range of analog functions can be implemented along with high performance digital contents on a single IC. This approach is called *System-on-Chip* (SoC), which even further improves the performance-to-cost ratio.

1.2 Motivation for Dissertation

With cost- and performance-effective CMOS technology, the concept of ubiquitous sensing and wireless communication with a micro-scale sensor device has shown high potential to be utilized in military, commercial, and medical applications. Depending on applications, different kinds of physical phenomena such as pressure, brightness, and temperature should be observed. However, most of the micro-scale sensors share the same fundamental objective, which is to observe inconspicuous yet meaningful data without disturbing their surroundings both physically and operationally.

To conform to the underlying non-obtrusive attribute, wireless sensor nodes should guarantee an extended period of life cycle while restricting the physical footprint. As the total amount energy that can be integrated on the system is limited, the core functional blocks have to be extremely energy efficient.

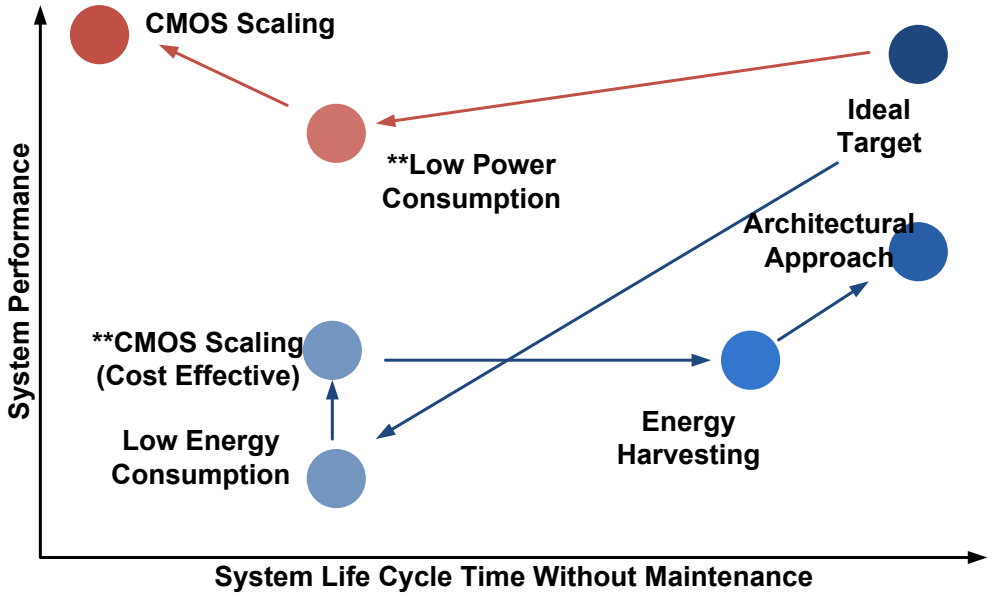


Figure 4: Design goals for wireless sensor devices considering performance and system life cycle.

The trade-off between system life cycle without any maintenance and system performance for wireless sensor devices is shown in Figure 4. The ideal goal is to have high performance and virtually infinite operating cycle, which is not realistic. In reality, as the overall energy budget is limited, both the system performance and the operation time of a wireless sensor are far off from the ideal target. This can be compared to a conventional high performance portable devices such as laptops or smart phones, which have higher computing power or higher system performance but last only about a day or couple of hour; a low energy consumption wireless sensor device should last over weeks or even years without maintenance. To improve the system life cycle without degrading the system performance, energy harvesting features can be added. In addition, through novel architectural approaches and the improvement in CMOS technology, the system performance might be enhanced.

Although the active power consumption of digital circuits can benefit from aggressive CMOS scaling, increased leakage currents will cancel out the overall efficiency gain. For low duty-cycled systems, leakage currents can have a huge impact on the

overall energy consumption [33]. Therefore, the conventional energy reduction approaches that are effective on high performance digital blocks cannot utilized in the sensor design; energy-efficient architectural schemes and circuit topologies should be devised. Restricting the overall energy budget in a sensor device inevitably degrade the system performance: the upper bound of communication distance, operation speed, and processing accuracy. If a large number of devices are deployed, the individual performance degradation can be compensated [37].

Sensor devices are usually deployed where the operating environment changes unpredictably. For example, changes in communication distance or device orientations would attenuate or intensify incoming and out-going signals. Consequently, unless these kinds of inevitable variations are compensated, a wireless sensor device would over-consume unnecessary energy for a given taks or under-consume too little energy to meet the requirement. Therefore, the operating efficiency will be different from the originally targeted value. For more reliable and accurate monitoring data, the ability to evaluate environmental changes is also required to fulfill the non-obtrusive operation.

The objective of the proposed research is to analyze and develop energy optimized design techniques that can improve the operating efficiency for a wireless sensor device in CMOS technology. To enhance the operating efficiency, each functional blocks in a system should focus on energy conservation while achieving the required tasks. In addition, variations in the operating condition should be properly observed and compensated. Otherwise, a wireless sensor device would consume unnecessary energy for a given task or too little energy to meet the requirements. Throuout the research, the two aspects for the efficiency enhancement will be analyzed, and a number of techniques that can fulfill the objective will be discussed. The contributions of this research will be as follows:

- Key functional blocks in a wireless sensor device, which can share common

design strategies in CMOS technology will be defined: the signal processing unit, the memory unit, and the power unit.

- Design challenges regarding low power signal processing will be analyzed, and a subthreshold analog computation system for ultra-low power analog signal processing will be demonstrated.

- A novel fully-gated ground 10T-SRAM cell that can reduce data dependent leakage currents for robust and energy-efficient operations will be presented.

- Possible energy sources for wireless sensor applications will be investigated.

- For inductively-coupled wireless power transmission, CMOS rectifier topologies will be discussed, and the charge leakage issues will be analyzed.

- A semi-active rectifier that can reduce the charge leakage and provide higher voltage conversion efficiency compare to conventional CMOS rectifier will be presented.

- A novel link-variation sensing technique that can evaluate operational disturbances such as component mismatches and displacement variations will be introduced, and the power receiver prototype with the proposed sensing technique will be demonstrated.

1.3 Organization of Dissertation

This dissertation consists of seven chapters.

Chapter 2 discusses design requirements and challenges for wireless sensor devices. Critical design constraints and system budgets are reviewed. For a generalized physical architecture of a wireless sensor device, common functional blocks that can share energy-optimized techniques in CMOS technology are discussed.

Chapter 3 explains the underlying motivation for low power signal processing for wireless sensor applications. To be extremely efficient in terms of energy consumption, analog signal processing concept is introduced. After discussing the operation of CMOS transistors in subthreshold region, the translinear loop is applied to subthreshold CMOS transistors to obtain a linear multiplication function. For a feasibility prototype, a current-mode matrix determinant computation system is implemented in 0.18 μm CMOS technology utilizing the tranlinear multiplication blocks and current-domain addition and subtraction blocks.

Chapter 4 discusses memory units for wireless sensor nodes. The basic operation of the static random-access (SRAM) memory cell is explained. In particular, the data-dependent leakage currents are discussed for robust SRAM read operations. The data-dependent leakage behaviors of differential SRAM cells are compared, and a fully-gated ground 10T SRAM cell that can substantially reduce the data-dependent leakage currents is introduced. The proposed cell is configured in a 45nm CMOS silicon-on-insulator (SOI) process along with other differential cells to demonstrate its ability to integrate a large number of cells without consuming additional energy.

Chapter 5 starts with possible energy sources for wireless sensor applications including variety of energy extracting methods. Among the energy candidates, inductively-coupled link is explained in detail since inductively-coupled link can potentially be used for energy transfer as well as data transfer. To convert electro-magnetic energy into electro-static energy, a AC-to-DC conversion circuit, otherwise known as a rectifier, has to be followed by an inductive link. As we are focusing on CMOS technology, CMOS full-wave rectifier topologies are discussed, and the charge leakage problem in a cross-coupled CMOS rectifier is analyzed. To allegviate the charge leakage issue, a semi-active CMOS rectifier is proposed to achieve higher voltage conversion efficiency.

Chapter 6 introduces challenges regarding unpredictable operation condition changes

after sensor deployments. As variations in operating conditions will inevitably degrade system efficiency, a proper link-variation sensing technique is required. A non-interruptive link-variation sensing scheme is proposed. To test the feasibility of the proposed technique, a inductively-coupled power receiver with a rectifier and the proposed link-variation sensor is implemented and tested.

Chapter 7 concludes this dissertation with a discussion on the future works.

CHAPTER II

WIRELESS COMMUNICATION AND UBIQUITOUS SENSING

2.1 Wireless Sensor Device

The fundamental motivation of the wireless sensor device is to sense and interact with surrounding physical phenomena in non-obtrusive manner. In implementing wireless sensor devices, two things have to be guaranteed for the non-obtrusiveness. A sensor should be operational for an extended period without any maintenance, and its physical footprint should remain inconspicuous.

As shown in Figure 5, the two critical requirements, the long-lasting feature and the small physical footprint, cannot be met simultaneously without any trade-offs. In order to achieve extended period operations, a wireless sensor should restrict overall energy consumption. Low energy consumption should be distinguished from low power consumption. As energy consumption is a product of power consumption and the corresponding duration, low-power consumption does not always guarantee low-energy consumption. For the ideal case, a device should consume as low power as possible to complete given tasks while minimizing the leakage power consumption for the rest of the inactive period.

High capacity energy sources are always desired for both enhanced operation time and performance. However, the small physical footprint requirement does not allow to integrate excessively large amount of energy sources. To maximize a dedicated volume for energy sources, high power density Li-Ion batteries and high energy density fuel cells are integrated together; Li-Ion batteries can supply energy for instantaneous high power demanding jobs and while fuel cells can be used to recharge Li-Ion batteries

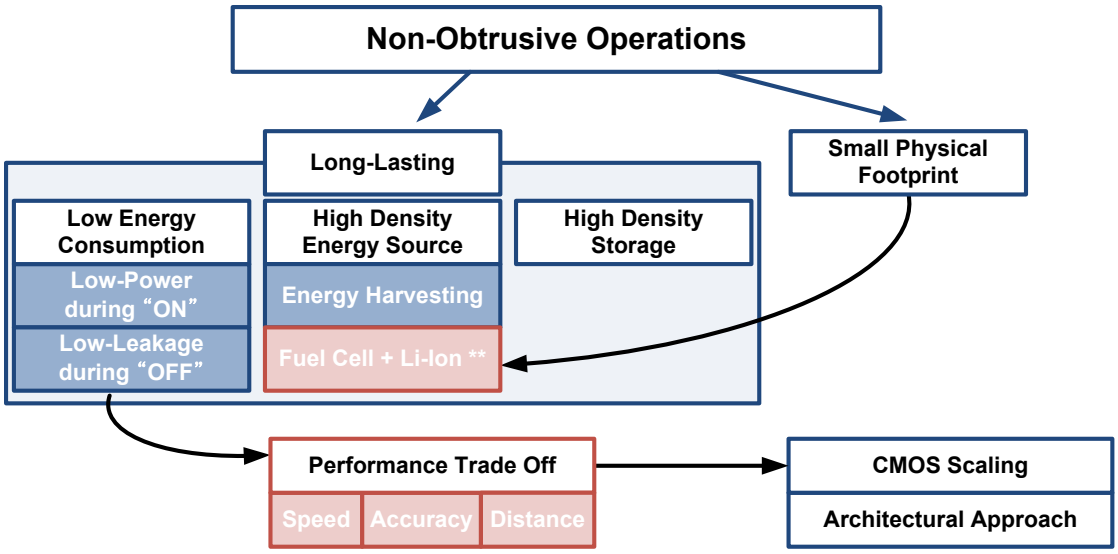


Figure 5: Motivation and design challenges for wireless sensor devices.

during low-power demanding situations. When there are appropriate ambient energy, energy harvesting can be added to provide virtually infinite amount of energy density.

Finally, for the long lasting feature, a high capacity memory block is required to store monitored data until they can be transferred to a base unit. As the CMOS gate length shrinks, a larger amount of memory cells can be integrated so that the overall storage capacity per silicon real estate increases. However, as the increased leakage currents in the advanced CMOS technology is inevitable, without any leakage reduction techniques, high density memory blocks implemented in deep submicron technology migh not be suitable for wireless sensor applications.

In the system performance perspective, operating speed, processing accuracy, and communication distance must be sacrificed for the low energy consumption demand. This is justified because it is more important to have a low-performance sensor that lasts very long time. As we will be leveraging CMOS technologies, we might expect to have benefits from CMOS scaling. A numerous functions can be integrated into a single chip, and the implementation cost decreases so that a number of CMOS based sensors can be deployed. Energy-optimized architectural and circuit approaches can be further introduced to break the performance versus energy consumption trade-off

circle.

2.1.1 Wireless Sensors in Bioimplantable applications

There are numerous on-going researches on biomedical area [27]. Among these, the applications associated with implantable sensing and stimulating devices have a strong correlation with low power integrated circuit techniques. Neural signal recording sensors, neuromuscular stimulation sensors, cochlear implants, retinal prosthetic device, vital signal monitoring implants are some examples [49][41][31][28]. Regardless of the purpose of these applications, their size should be small and the operation time should last as long as possible. In some applications, such as pace makers, batteries are implanted together. However, batteries always have possibilities of hazardous malfunctions and require replacement. The other method, external wired power connection, would provide stable power for a long period of time but may cause infection [45][44]. Thus, wireless powering from external units is strongly desired [21].

The amount of power that can be transmitted to implanted device should be less then $10\,\mathrm{mW/cm^2}$ due to biological safety. Inductive coupling, a popular power link method, inherently suffers from low power transfer efficiency to two degraded coupling coefficient and quality factors of transformers. Consequently, low power circuit design becomes a critical issue to optimize the limited available power.

These bio-implantable devices sense targeted signals from targeted organs or stimulate organs with appropriate electrical pulse. In doing so, at least one way data transfer should be established and bi-directional data transfer would enhance accuracy and versatility of the system. Wired connection is an easy way to establish communication link but as in the wired power connection, may have infection problems. Thus, wireless communication link is required [20][19]

Figure 6 represents generalized biomedical implantable device operating without batteries [18][16]. Power and data are provided from the outside control unit which

does not suffer from limited power and size. Once the incoming signal received at the implanted unit, the rectifier generates coarsely regulated DC voltage and the voltage regulator produce appropriate supply voltage for the implanted system. The incoming signal also contains control signals and data for stimulation and sensing. Once, a certain voltage level is reached, other circuit modules are ready to operate. The data recovery block extracts incoming data and toss them to the low power signal processing block [29].

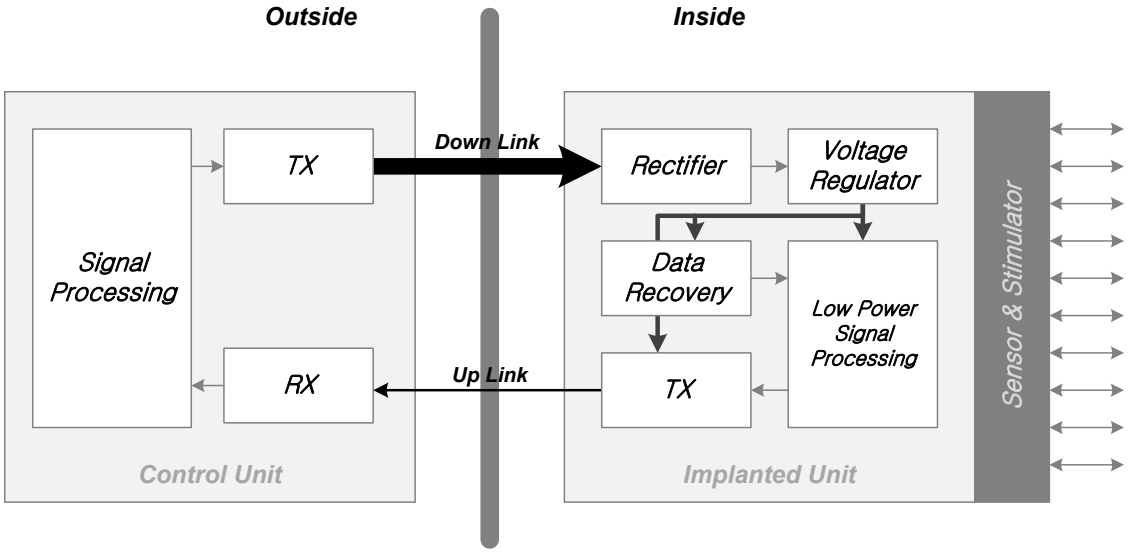


Figure 6: Generalized battery-less implantable sensor system.

If there is unlimited power and space, a powerful DSP core can be integrated. However, severe constraints on power and size force us to utilized ultra low power and simple signal processing architecture. Depending on the purpose, this low power signal processing block is uniquely designed to provide appropriate signal conditioning while compressing data as compact as possible to reduce the required data rate; high data rate cannot be accommodated due to power consumption [14]

Limited power is also problematic in transmitting block. Transmitter is a power hungry block and we do not have luxury for conventional transmitters. The most efficient way to transmit signals is "Load Shift Keying" (LSK). Data is modulated on

the loading condition at the implanted side, thus power can be saved. However, LSK suffers from data rate. For some neural sensing applications where about 10Mbps data rate is required, active transmitters are used [21][1].

Issues

- **Integration**

  The implanted unit should be as compact as possible. Generally, inductor coils for communication link and capacitors for voltage regulations cannot be integrated [44].

- **Data rate**

  To increase data rate, the carrier frequency and the power consumption should increase. However, higher frequency and higher power increase biological damage risks. Thus, the data rate, frequency, overall power consumption should be carefully selected.

- **Bio safety**

  After all, all the design constraints originate from bio safety: frequency, power consumption, size, and data rate.

2.2 Key Design Specifications

Low maintenance wireless sensor devices are useful in a wide range of applications. Before explaining some of the design approaches of the core circuit blocks, it is appropriate to discuss the key design specifiactions for the essential blocks other than the core circuits: the type of the sensing unit, the maximum allowed physical dimension, the type of the energy source, the communication distance, and the power consumption level. The main guide line of the key design specifications stems from applications, and the design specifications are closely correlated as shown in Figure 7.

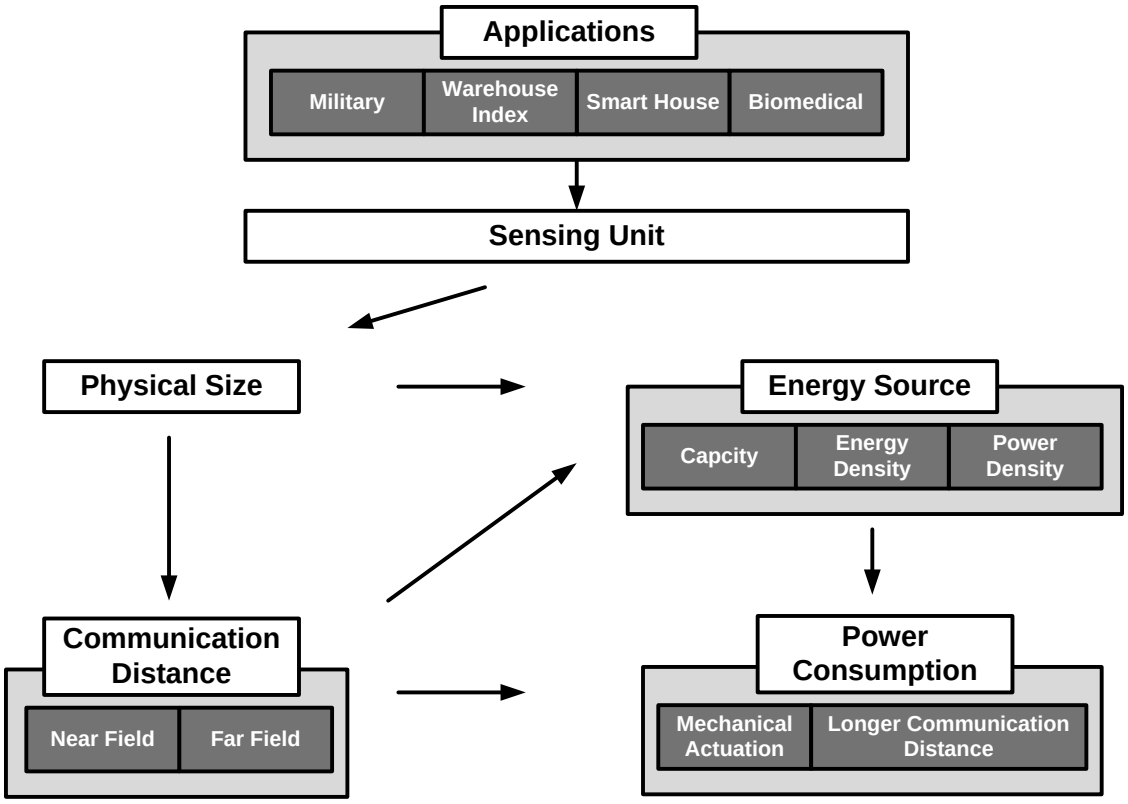


Figure 7: Key design specifications for wireless sensor devices.

Wireless sensor applications can be divided by applications: miliatary fields, smart house, warehouse indexing, and medical fields. The sensing unit has to be chosen by the application needs. As the sensing unit is rarely realized with a standard CMOS process, the sensing unit and the rest of the functional blocks often form a system-in-package module. The non-CMOS fabrication of the sensing unit would increase the overall implementation cost, and serious efforts have to be put on the integration of the sensing unit to comform to the small physical footprint feature.

The overall physical footprint has to be regulated depending on the application requirements as well. One of the major key players in determining the physical dimension is the operating frequency. For the applications in which high frequency wireless data/power transmission is prohibited, the near field electromagnetic radiation is utilized; for biomedical fields, the amount of transmitted wireless power is restricted at high frequencies due to safety issues. The radiation is considered to be

the near-field radiation if the communication distance is within the wavelength of the wireless frequency. Inductive coupling is often used for the wireless sensors that utilize the near field radiation, and the overall physical footprint is limited by the volume of the coupling inductors. On the other hand, if the communication distance is over two wavelengths apart, the radiation is called the far field radiation. For the far field, various antennas can be used, and the form factors for the antennas are inversely proportional to the wireless frequency. Therefore, the physical footprint can be reduced if higher frequency is chosen. However, the higher operating frequency a sensor utilizes, the more energy has to be consumed in the peripheral circuit blocks.

As mentioned briefly in the previous section, high capacity energy sources can break the performance trade-off circle by providing more margin on the energy consumption side for improved performance without reducing the operation time. However, as high capacity energy sources increases the overall physical dimension as well as the implementation cost, they cannot be always accomodated. While the capacity of the energy source has a direct impact on the physical appearance, the characteristic of the energy source affects the power consumption level. Energy sources show different characteristics in the energy density and power density. Most of the time wireless sensor devices do not require a power demending situation so that energy sources having high energy density are preferred. However, transmitting data over wireless channels, stimulating a target with high voltage pulses, or actuating any mechanical parts would require power demanding loading conditions.

2.3 Micro-Scale Wireless Sensor Device in CMOS Technology

2.3.1 Essential Circuit Blocks

Figure 8 shows a generalized essential block diagram of a typical wireless sensor. Each sensor device is equipped with an application-oriented sensor unit that translates targeted physical phenomena into electrical signals. In addition, the design of

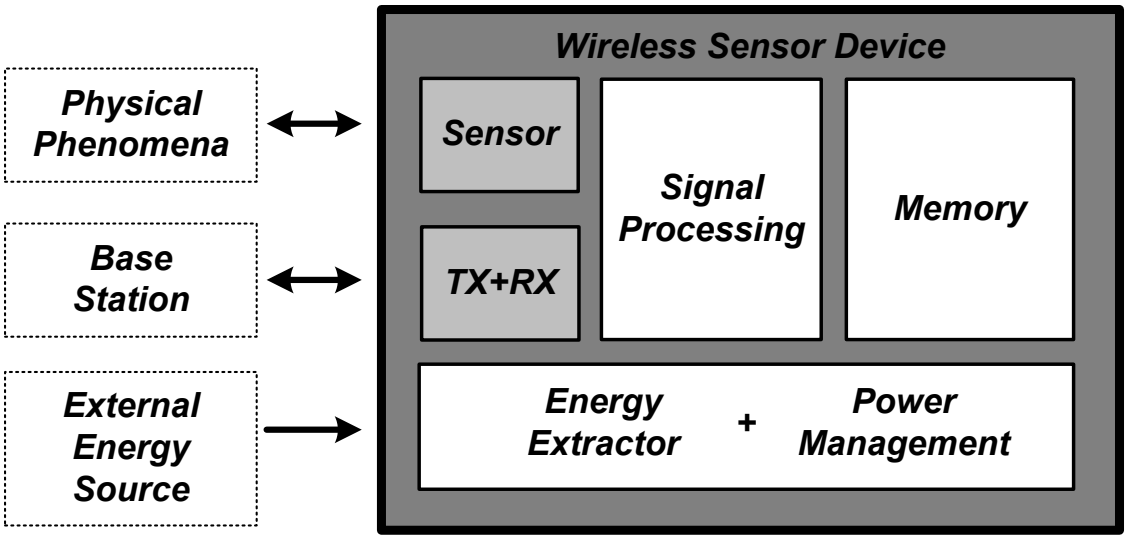


Figure 8: Diagram of a generalized wireless sensor device.

a transceiver block heavily depends on the application. For example, short-distance sensors utilizes "load-shift keying" as it does not require a power-hungry power amplifier; in the near field radiation, any impedance changes at the receiver side are reflected at the trasmitter side.

After the external information is handled in and out of the application-oriented front ends - the sensor unit and the transceiver unit, the electrical signals are conditioned by a signal processing unit, and the processed data are stored in a memory unit. From the energy management perspective, the physical dimension of a wireless sensor restricts the total amount of energy that can be carried along while the operating mechanism of a wireless sensor does not allow to exchange integrated energy sources on a periodic basis. Therefore, it is highly preferred to have an energy extractor that can harvest energy from external energy sources [38]. The signal processing unit and the memory unit should focus on energy conservation rather than performance improvement; the data rate and accuracy can be sacrificed for lower energy dissipation.

2.3.2 Benefits and Chanllenges in CMOS Technology

A much as CMOS technology brings a number of advantages to modern electronic systems, the advanced CMOS technology can also help improving the performance of the essential circuit blocks in wireless sensor devices - the signal processing unit, the memory unit, and the energy management unit with low power, low cost and supporting multiple functions. Therefore, it is natural for the essential blocks to be fabricated with CMOS technlogy.

The three blocks are not totally new concepts. They are also widely used in portable electronic devices. The signal processing unit is a mixed-signal system in which both analog and digital circuits co-exit. The memory unit consists of digital blocks while the energy managementment unit contains mostly analog circuits. While CMOS technology has brought direct benefits to digital circuits by improving speed and reducing area and power consumption, it is debatable whether standard CMOS technology has evolved in favor of analog and mixed-signal circuits. However, as most of information processing is done in digital domain, even if the performance of the non-digital side degrades, enhancing the digital side would increase the overall system performance. If we compare the state of the art smartphone with a cell phone back in the early 2000's, it is evident CMOS technology has had possive impacts. For wireless sensor applications, CMOS technology has provided the feasibility to integrate multiple functions with low power and low cost.

Since wireless sensor devices should be operational for an extended period of time, the active circuit blocks should be energy-efficient. Energy consumption has to be distinguished from power consumption. A system can be low power but it does not necessarily imply that the overall energy consumption of the system is low. Energy consumption is an integration of power consumption over a given period. In order to achieve extended period operations, the active circuits in a wireless sensor should maintain low-power consumption not only performing meaningful jobs but also being

in a stand-by mode.

Although the active power consumption of digital circuits can benefit from aggressive CMOS scaling, increased leakage currents will cancel out the overall efficiency gain, which will be further degraded for low-duty-cycle systems [33]. Therefore, the energy reduction cannot fully rely on the technology development; efficient systematic schemes should be devised. In the meantime, reducing energy consumption of a sensor device inevitably lowers the upper bound of communication distance, operation speed, and processing accuracy. If a large number of devices are deployed or the available energy for an individual sensor is increased, the performance degradation can be improved [37].

Sensor devices are usually deployed where the operating environment changes unpredictably. For more reliable and accurate monitoring data, the ability to adaptive to environmental changes is also required to fulfill the non-obtrusive operation.

CHAPTER III

LOW POWER SIGNAL PROCESSING

Gene's law states that CMOS scaling would reduce power consumption per signal processing task. The roadmap in Figure 3 [26] states that the operating efficiency of complex signal processing circuits will improve since signal processing demands will increase but the overall power consumption will tend to stay relatively constant; to be accurate, due to the side effects from CMOS scaling, the overall power consumption will eventually follow the processing demand curve unless novel fabrication techniques are introduced [33].

However, even if we ignore the possible side effects, the statement induced from Figure 3 is only valid for the systems that are active most of the time. In other words, the aggressive scaling improves the efficiency of the high-duty-cycled systems.

Active-power density and subthreshold-leakage power density are compared in Figure 9. As the gate length shrinks, standby power consumption that is proportional to subthreshold-leakage currents cannot be overlooked. Since wireless sensor devices operate at substantially low duty cycle, sole digital implementation of signal processing functions in those applications might not be feasible.

The adverse effect of the increased leakage power density becomes severe if we care about energy consumption. In particular, for wireless sensor devices, reducing the standby power consumption is critical in saving the limited energy resources. Figure 10 compares the duty cycles of high performance portable devices and wireless sensor devices to understand the effects of the reduced active power density and the increased standby power density on the overall energy consumption.

For high performance portable applications, the devices show high duty-cycle. If

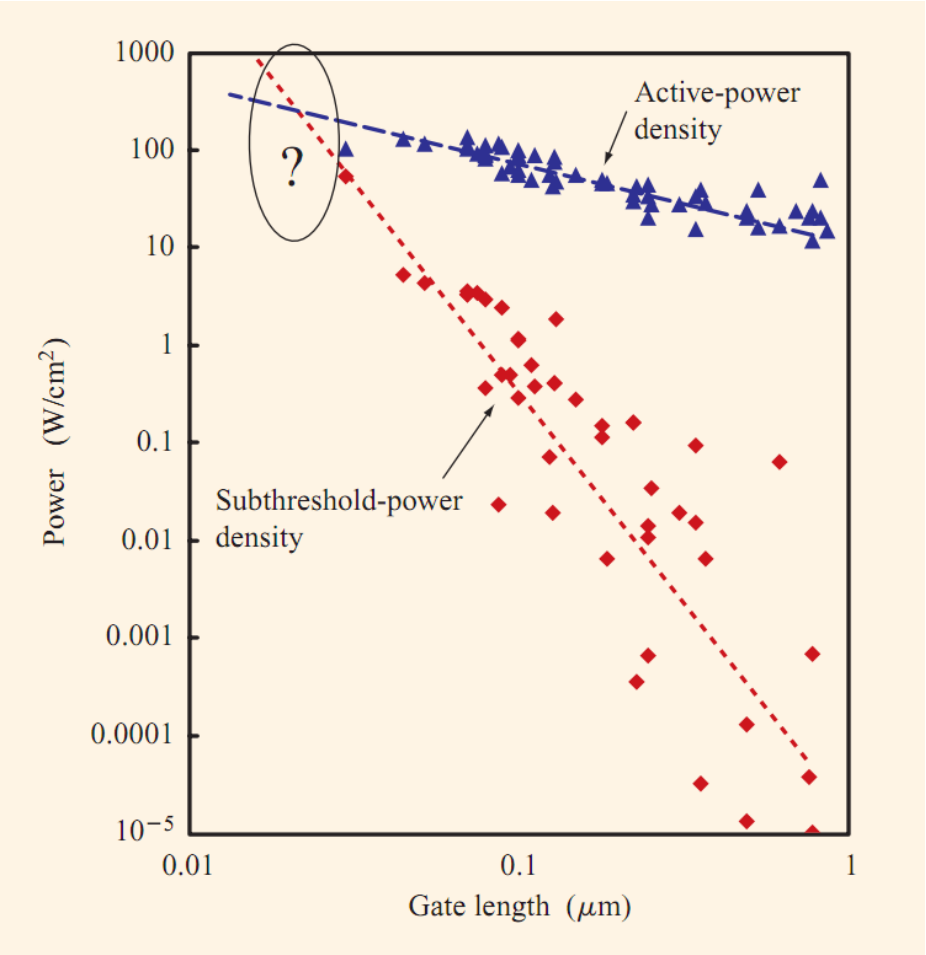


Figure 9: Active-power density and subthreshold-leakage power density trends and estimations versus gate [33].

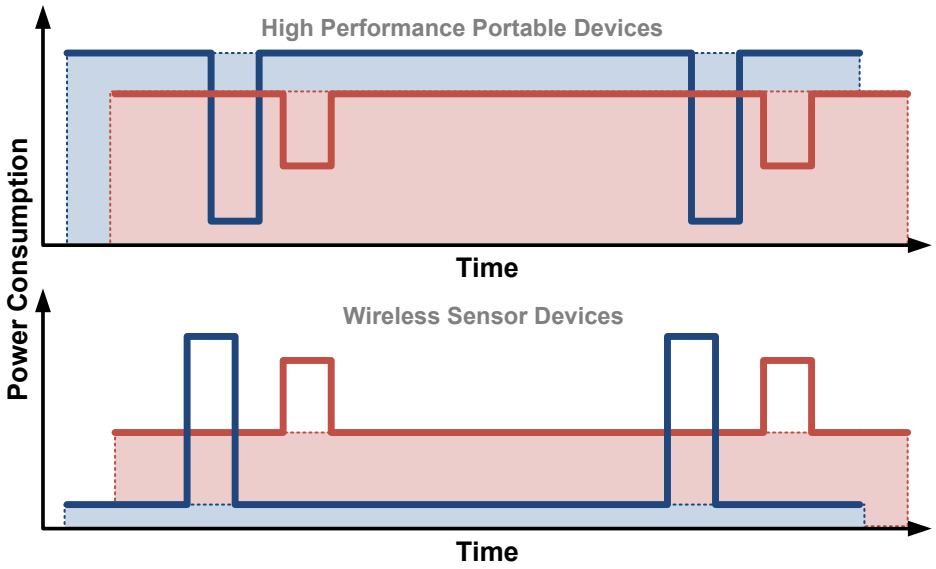


Figure 10: Duty cycle comparison between high performance portable devices and wireless sensor devices.

we are migrate from a long-channel CMOS technology to a short-channel technology, to perform a given amount of signal processing tasks, the active power consumption plays a dominant role in total energy consumption. Therefore, we can benefit from CMOS scaling.

On the other hand, for wireless sensor devices, where devices have extremely low duty cycle, if CMOS scaling is leaveraged just as the portable devices, we might end up with higher energy consumption due to increased leakage power.

3.1 Analog Signal Processing

When it comes to a realization of a signal processing function, digital implementation is a popular method since a sophisticated algorithm can be adopted. However, the performance of the digital system is directly related to the power consumption. For example, the quantization noise at the front analog-to-digital conversion and the round-off errors during the computations can be suppressed at the expense of higher data bits, which in turn increases the power consumption. Therefore, the digital-based approach might not be a feasible option in the applications where the power

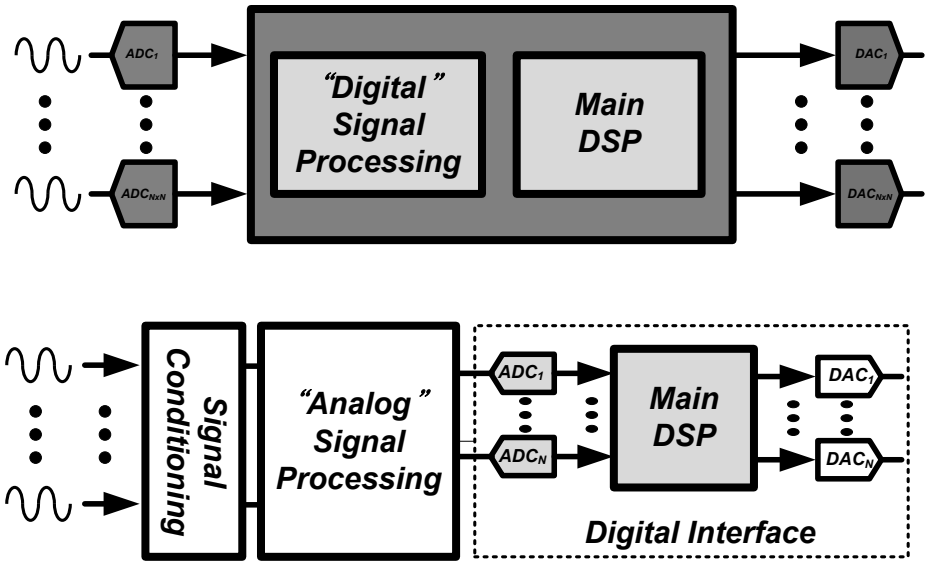


Figure 11: Implementation of signal processing with a digital approach and an analog approach.

consumption is strictly restricted.

Figure 11 compares the signal processing in the digital approach and the analog approach. Since the computations are performed in the analog domain, the burdens on the analog-to-digital conversions can be reduced. The analog signal processing blocks are compact in size and consume less power. Therefore, with the analog signal processing concept, virtually the same systematic functions as in the digital implementation can be realized with reduced system complexity.

For cognitive radio applications, a multi-resolution spectrum sensing (MRSS) technique has been implemented with the analog signal processing concept [35]. The MRSS technique relaxes the ADC requirements while its performance remains comparable to that of digital approach.

Similarly, a fully integrated analog matched filtering technique has been reported for radar applications [25]. In these applications, the conventional approaches require computationally expensive both fast Fourier transforms and inverse fast Fourier transforms. However, in [25], an analog multiplier, an analog integrator, and an arbitrary

waveform generator were combined to provide a power-efficient yet reconfigurable solution.

3.2 CMOS Transistors in Subthreshold

While some research efforts are focused on achieving high speed and complex functions, reducing the power and energy consumption is a key point in wireless sensor applications. In particular, when power and energy are restricted but speed is not much of a concern, the subthreshold operation would be the optimum choice [1]. In addition, for the portable systems that need sophisticated computing only for a short duration of time, we can use ultra-dynamic voltage scaling (UDVS), which allows the same circuit to operate at high voltage or high frequency for performance critical occasions and at subthreshold or low frequency for the rest of the time [2].

The energy and performance analysis in [3] shows that minimum energy is consumed in the subthreshold operation in the low-to-moderate performance. The main drawback of operating circuits in this regime is performance degradation. Due to limited currents and voltage, high speed circuit operations cannot be supported, and signal-to-noise ratio (SNR) decreases. In other word, the overall performance is sacrificed over power efficiency. Therefore, it is generally considered hard to apply the subthreshold techniques in high performance applications; their first priory used to be complex functionalities with high speed and high accuracy.

The intrinsic energy-efficient characteristics of the subthreshold design can be maximized if it is applied to the analog signal processing concept shown in Figure 11. Not only the power budgets on the digital interface blocks - analog-to-digital conversion and digital-to-analog conversion but also the analog domain power consumption will be drastically reduced.

Operating a transistor in the subthreshold region implies that the gate bias voltage is below the threshold voltage. To understand the subthreshold conduction, a NMOS

transistor is chosen. The source and the body of the NMOS are connected to the ground to eliminate the body effects for simplicity. The configuration is shown in Figure 12. When the gate voltage, V_G, is below the ground potential, the negative gate potential repells negative charges under the gate channel. This is called the accumulation region. As V_G increases above the ground potential, the gate potential starts to attract negative charges, which deplete the p-type gate channel. In the depleted region, there are not enough free electrons to generate drift currents. If the drain potential is above $4U_T$ or above 100 mV at a room temperature, the diffusion currents flows from the drain to the source due to the electron density gradient. This is called the subthreshold conduction, and the drain current depends exponentially on the gate-source voltage. As the gate voltage increases above the threshold voltage, the inverted channel full of free charges is formed under the gate area. If the channel is inverted, the transistor is in the strong inversion region; when $V_{DS} > V_{GS} - V_{TH}$, the transistor is in the saturation mode, and the drain current is proportional to square of the overdrive voltage.

To operation a digital circuits in subthreshold, the supply voltage should be below the threshold voltage either the supply voltage or the ground will be applied to the gates. In analog circuits, as transistors are often stacked in series, having diverse gate-source conditions and different threshold voltages due to the body effect, current densities rather than gate voltages have to be controlled to ensure the subthreshold operation.

As the first step for analog signal processing, if a CMOS transistor is biased at sufficiently low current-density, the transistor operates in the subthreshold region, where the gate voltage and the drain current show exponential relation. If the size of a transitor increases with the same amount of a bias current, the transistor falls into the subthreshold operation. Figure 13 plots the drain currents versus the gate voltages for different transistor sizes. The y-axis is in log-scale. If we look at the zoomed-in

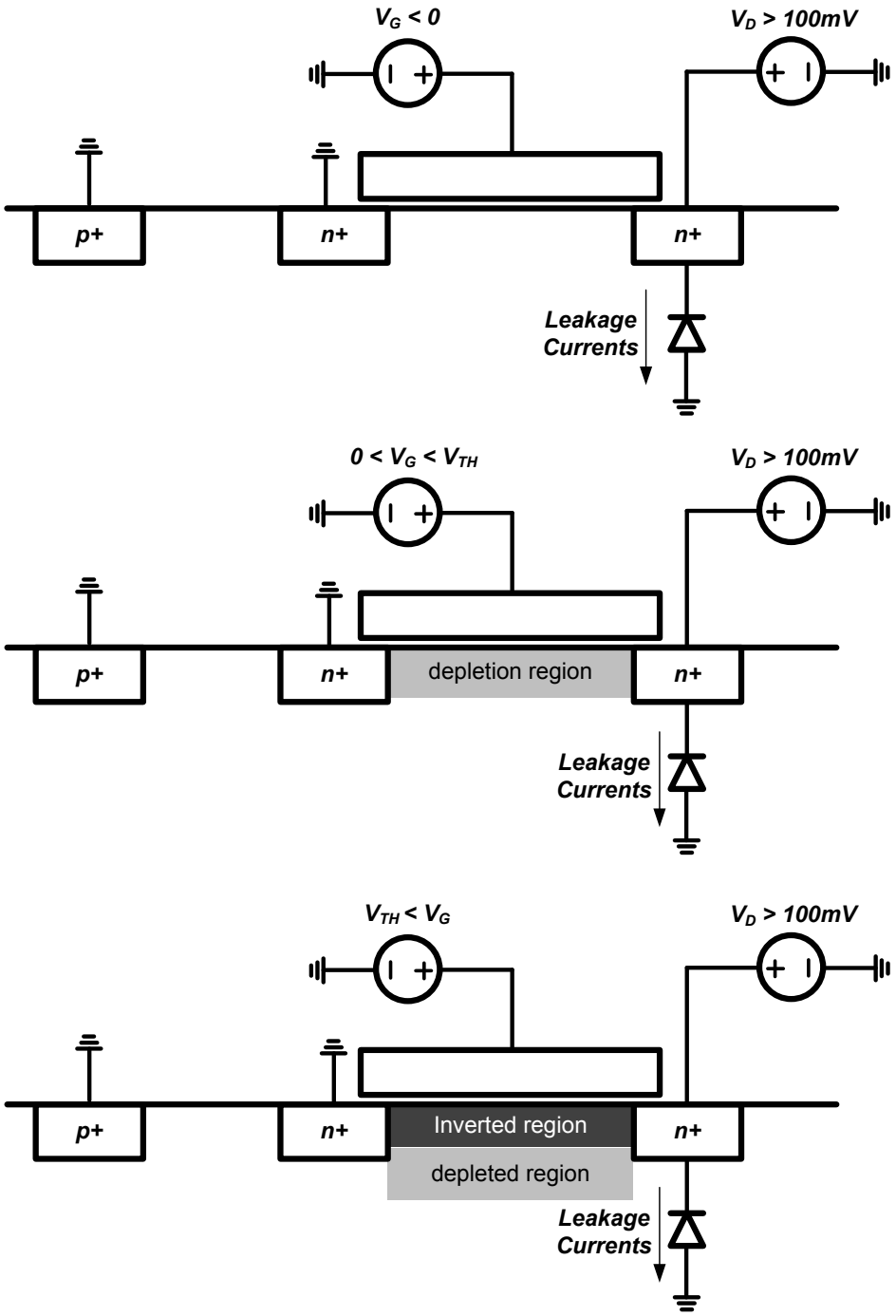


Figure 12: Changes in a NMOS channel as the gate voltage changes.

plot, as the current density increases, the operating region shifts towards the strong inversion region in which the exponential behavior is no longer valid. Therefore, unless current density is sufficiently suppressed, any analog processing blocks that depend on the exponential current behavior coult not produce valid outputs. Besides, the current density factor, device mismatches and parasitic leakage currents from parasitic diodes have to be considered to guarantee reliable outputs.

3.3 Current-Mode Arithmetic Computations for Analog Signal Processing

3.3.1 Translinear Principal and Key Building Blocks

For a transistor in subthreshold region, the gate and source voltages, V_G and V_S, and the saturated drain current, I_D, can be approximated to an exponential relation [11]:

$$I_D = 2\mu_n C_{ox} \frac{W}{L} \exp\left(\frac{V_G - V_{T0} - nV_S}{nU_T}\right) \tag{1}$$

If a translinear loop operates in the subtreshold region as shown in Figure 14, the voltage loop relation, $V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4}$, is translated into the current multiplication, $I_{D1} \times I_{D3} = I_{D2} \times I_{D4}$ as shown in (2)) and (3)).

$$\begin{cases} V_{GS1} = K_1 ln\left(I_{D1}\right) \\ V_{GS2} = K_2 ln\left(I_{D2}\right) \\ V_{GS3} = K_2 ln\left(I_{D3}\right) \\ V_{GS4} = K_1 ln\left(I_{D4}\right) \end{cases} \tag{2}$$

$$\begin{cases} V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4} \\ K_1 K_2 ln\left(I_{D1} \times I_{D3}\right) = K_1 K_2 ln\left(I_{D2} \times I_{D4}\right) \end{cases} \rightarrow \quad I_{D1} \times I_{D3} = I_{D2} \times I_{D4} \tag{3}$$

In order to represent a given value, X, in a differential current mode circuit, the X is normalized to the bias current, I_B. Then, the normalized value, $x = X/I_B$,

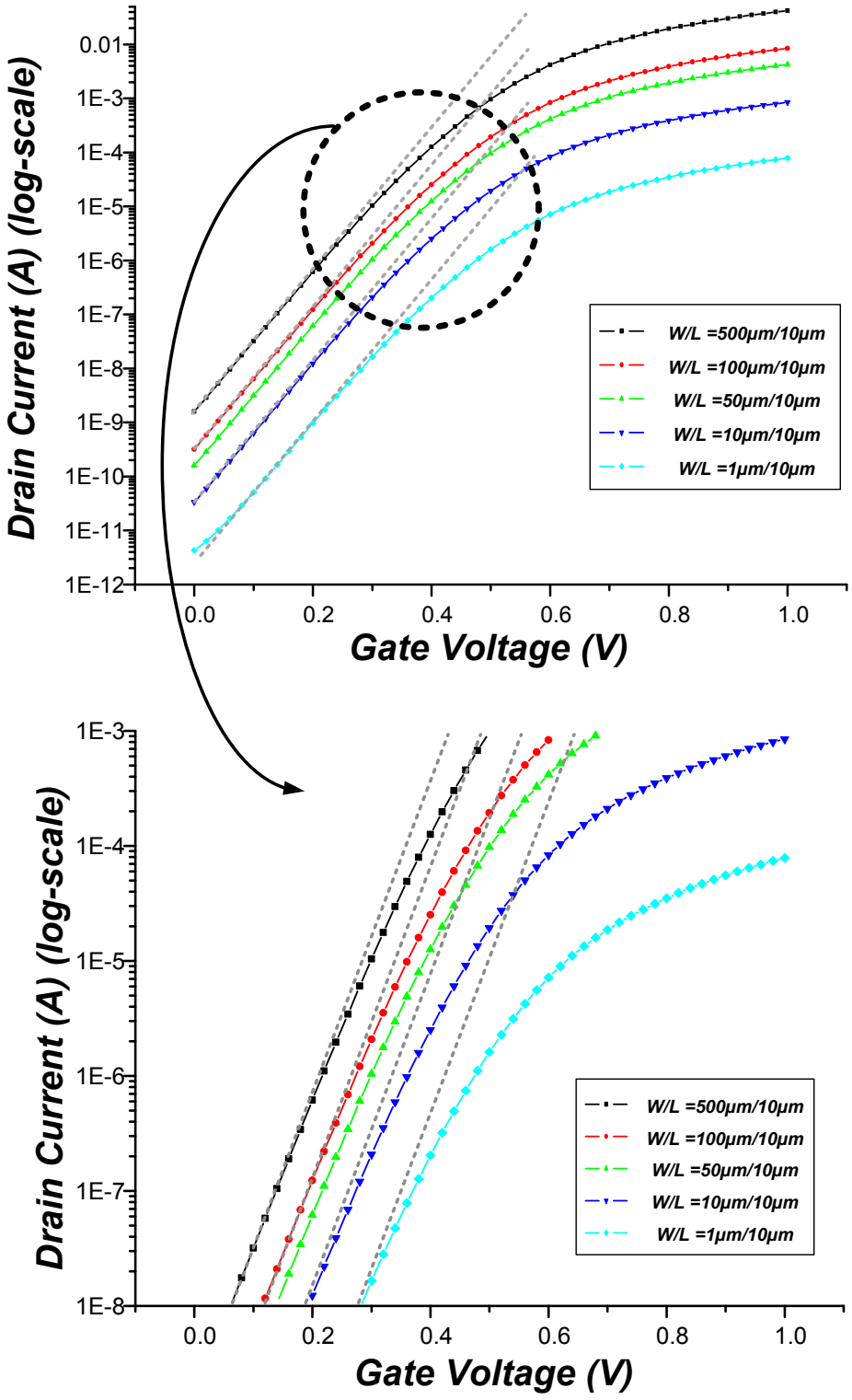


Figure 13: Changes in a NMOS channel as the gate voltage changes.

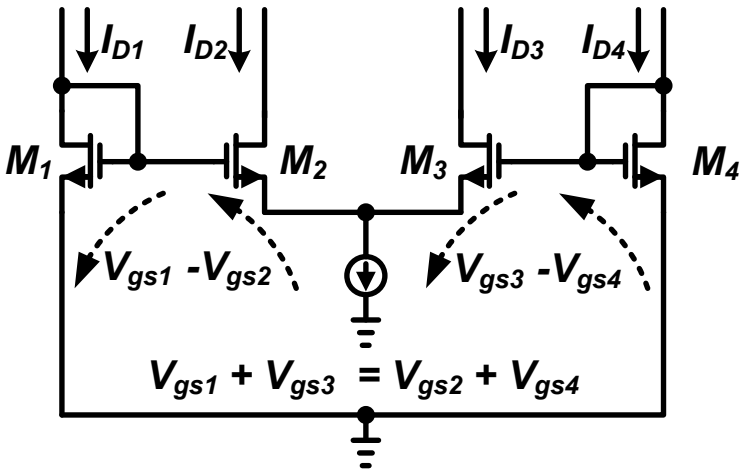


Figure 14: CMOS translinear loop operating in subthreshold.

is modulated onto the I_B (4). The modulated differential current signals can be represented as follows:

$$\frac{X}{I_B} = x \quad \rightarrow \quad I_B(1 \pm x) \tag{4}$$

In the digital implementation, the resolution of a given value is determined by the number of bits, which is restricted by the system power and area budget. In the proposed analog approach, on the other hand, the resolution is limited by circuit noise, linearity, and devices mismatch [22]. Therefore, design trade-offs and architectural ideas are necessary to minimize accuracy degradation.

In the proposed multiplier cell, the differential balanced architecture was adopted [17]. There are virtually four intertwined TL loops in Figure 15 to perform multiplications of differential signals as in (5) and (6). The outputs of the two translinear loops are summed to produce the final differential outputs as in (7).

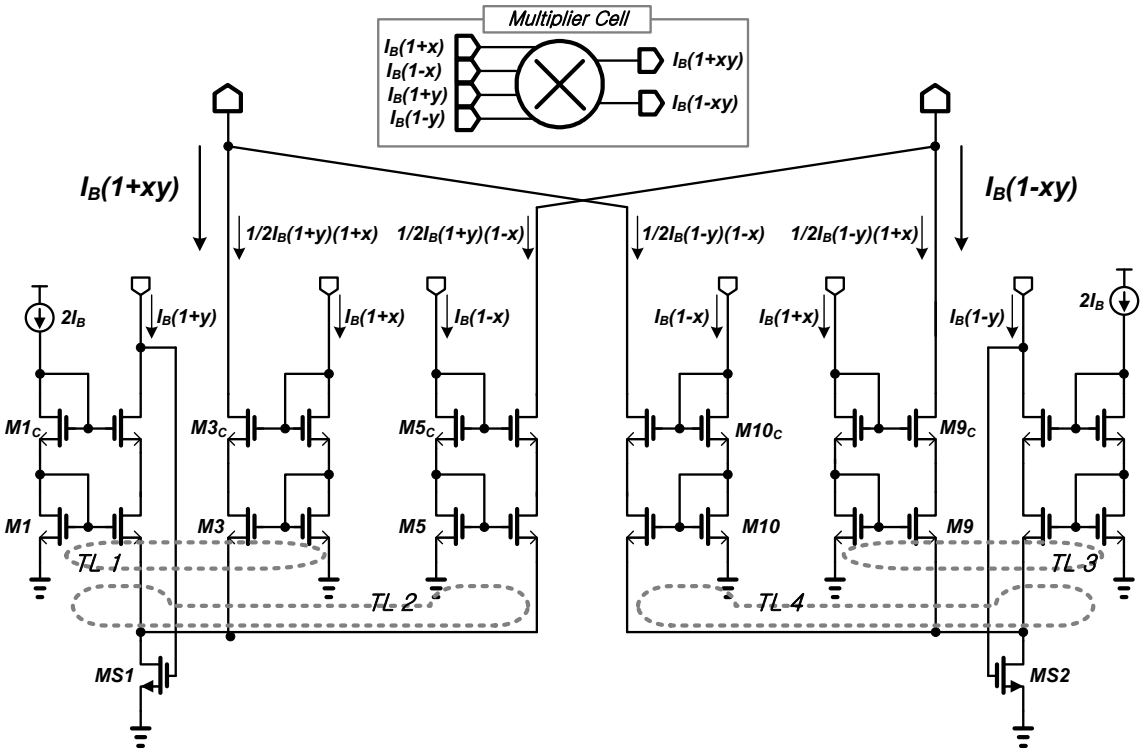


Figure 15: Cascode differential balanced current-mode multiplier using translinear loops in the subthreshold region.

$$\frac{I_B(1 \pm x) \times I_B(1+y)}{2I_B} = \frac{I_B(1 \pm x + y \pm xy)}{2} \tag{5}$$

$$\frac{I_B(1 \pm x) \times I_B(1-y)}{2I_B} = \frac{I_B(1 \pm x - y \mp xy)}{2} \tag{6}$$

$$(5) + (6) = I_B(1 \pm xy) \tag{7}$$

The differential architecture has strong advantages. First, it rejects common-mode noise. Second, both positive and negative values can be easily expressed, while expressing negative terms would be difficult without using negative supplies in a single-ended architecture.

However, the (5) and (6) relations are vulnerable to device mismatch and channel length modulation. The forward current mismatch (8) in a current mirror can be approximated to the functions of G_m, I_F, $\triangle V_{T0}$, and β, which denote the gate transconductance, the forward current, the variation in threshold voltages, and the

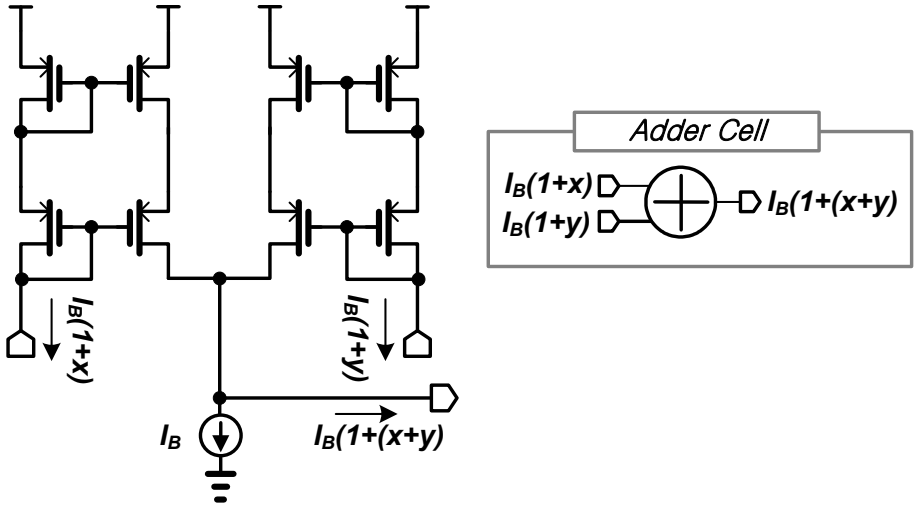


Figure 16: Current mode adder cell.

transconductance factor, respectively [11].

$$\frac{\triangle I_F}{I_F} = \frac{\triangle \beta}{\beta} - \frac{G_m}{I_F} \triangle V_{T0} \tag{8}$$

Given a device mismatch condition, the G_m/I_F factor should be minimized to reduce the impact of the threshold variation on the current mismatch in (8) and this implies increasing bias currents. However, as the currents increase, the transistors go into strong inversion regime, in which (1) is no longer valid. Thus, the device sizes should also be increased accordingly for the transistor to stay in subthreshold region.

In addition, for a transistor in subthreshold operation, both the source and drain voltages contribute to the channel length modulation. In the proposed multiplier cell, the sizes of the tail transistors, $MS1$ and $MS2$, in Figure 15 are increased to reduce source voltage variations and the cascode-configuration was used to minimize drain voltage variation. Finally, since the process variation in general is proportional to area [22], the minimum transistors are avoided.

Since all the signals are in a current mode differential form, one adder cell in Figure 16 can perform addition in (9) and subtraction in (10) by summing up currents in either direction.

$$I_B(1 \pm x) + I_B(1 \pm y) - I_B = I_B(1 \pm (x + y)) \tag{9}$$

$$I_B(1 \pm x) + I_B(1 \mp y) - I_B = I_B(1 \pm (x - y)) \tag{10}$$

3.3.2 Matrix Determinant Computation

The computations involving matrices play essential roles in a number of signal processing applications [10]. The determinant computation is one of the most widely used functions in matrix computations that can be easily applied to wireless sensor applications. As an example of the signal processing unit, a matrix determinant computation system has been designed.

Since the multiplier cells and adder cells are efficient in power and area consumption, the analog domain implementation allows to use multiple of the arithmetic cells. Thus, a 2-by-2 determinant and 3-by-3 determinant can be computed directly as in (11) and (13).

$$\begin{aligned} \left|\mathbf{A}^{2\times 2}\right| &= \begin{vmatrix} I_B(1 \pm a_{11}) & I_B(1 \pm a_{12}) \\ I_B(1 \pm a_{21}) & I_B(1 \pm a_{22}) \end{vmatrix} \\ &= I_B(1 \pm \mathbf{D_2}) \end{aligned} \tag{11}$$

$$\mathbf{D_2} = a_{11}a_{22} - a_{12}a_{21} \tag{12}$$

$$\begin{aligned} \left|\mathbf{B}^{3\times 3}\right| &= \begin{vmatrix} I_B(1 \pm b_{11}) & \cdots & I_B(1 \pm b_{13}) \\ \vdots & \ddots & \vdots \\ I_B(1 \pm b_{31}) & \cdots & I_B(1 \pm b_{33}) \end{vmatrix} \\ &= I_B(1 \pm \mathbf{D_3}) \end{aligned} \tag{13}$$

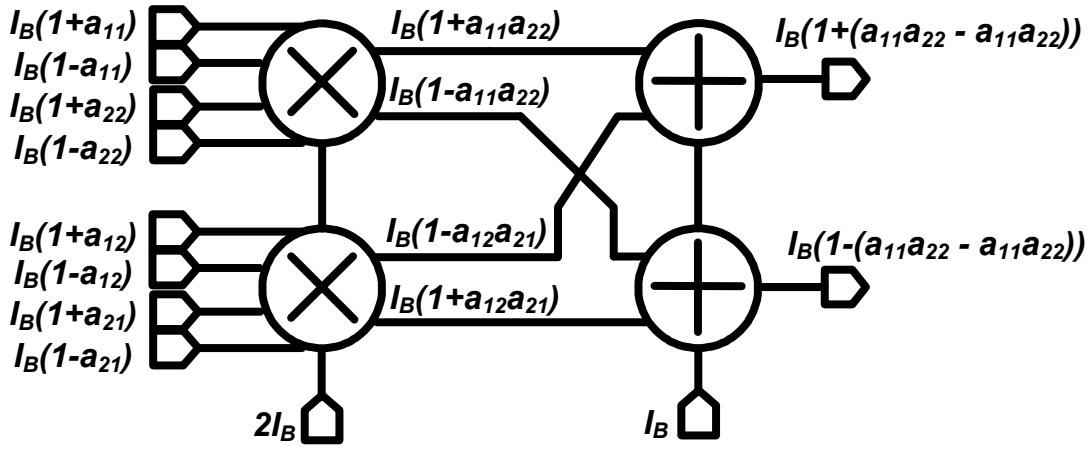


Figure 17: Diagram of the 2-by-2 determinant cell.

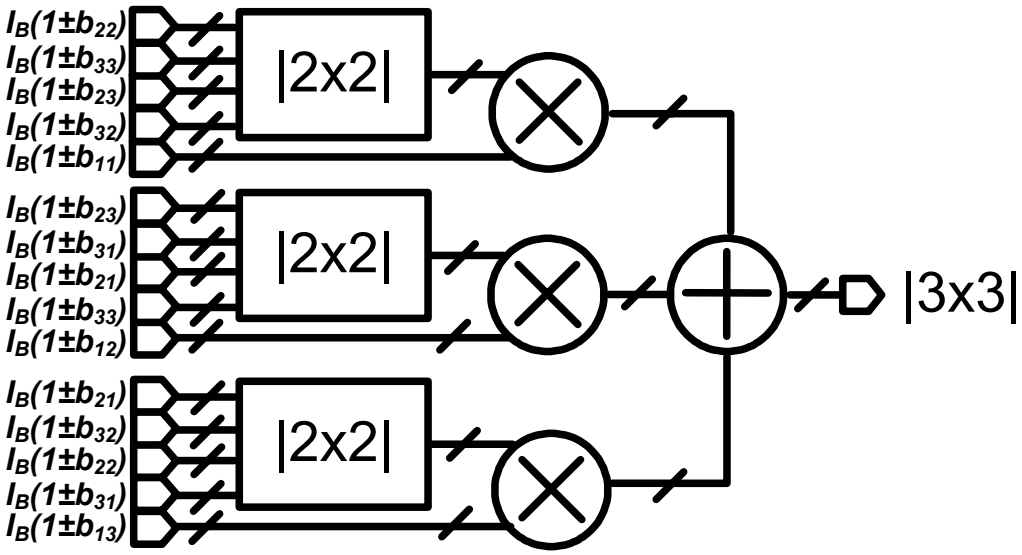


Figure 18: Diagram of the 3-by-3 determinant cell.

$$\begin{aligned}\mathbf{D_3} = b_{11}(b_{22}b_{33} - b_{23}b_{32}) + b_{12}(b_{23}b_{31} - b_{21}b_{33}) \\ + b_{13}(b_{21}b_{32} - b_{22}b_{31})\end{aligned} \tag{14}$$

The 2-by-2 determinant cell is a mere combination of two multiplier cells and one subtraction in Figure 17. The 3-by-3 case uses three 2-by-2 determinant blocks followed by multiplication and summation in Figure 18.

3.3.3 Experimental Results

Since the proposed circuit is operating in current mode, a voltage-to-differential current converter is implemented for test purposes as shown in Figure 19. The two identical voltage feedback loops set up the input voltage, V_{IN}, and the reference voltage, V_{REF} involving subthreshold operational amplifiers and an external resistor, R, can generate input differential currents. When R is set to $1/I_B\,(\Omega)$, $V_{IN} - V_{REF}$ becomes the modulation index so that the differential current, $I_B(1 \pm (V_{IN} - V_{REF}))$, is generated.

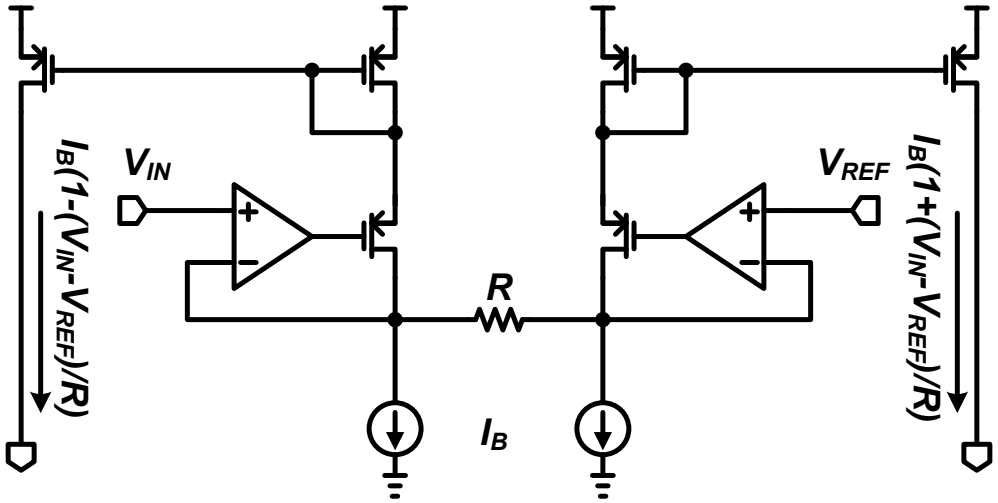


Figure 19: Diagram of the voltage-to-differentail current converter.

The overall system architecture is shown in Figure 20. The system was implemented in a TSMC 0.18 μm CMOS process. The total size is 560 μm $\times$ 680 μm, which includes a 2-by-2 determinant cell, a 3-by-3 determinant cell, biasing circuits, and the V-I convertors. The die photograph of the test chip is shown in Figure 20. The bias current, I_B, can be calibrated with the binary weighted 5 bit selection signal (S<0:5>). The range of the input voltages ($V_1 \sim V_9$) are set to 0.2 $\sim$ 1.2V with a 1.8 V supply and the V_{REF} and the R are set to 0.7 V and 10 MΩ, respectively so that the range of the modulation index is ranging from -0.5 to $+0.5$.

To evaluate the performance of the 2-by-2 determinant over a wide range, the

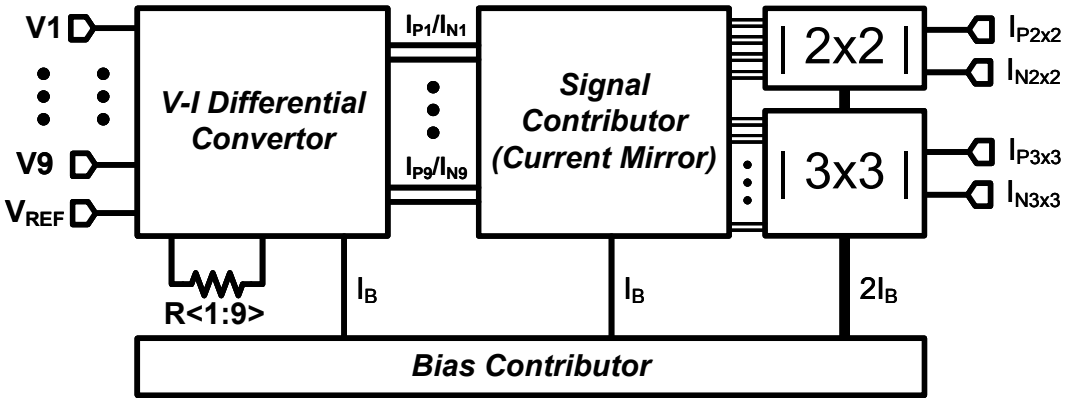


Figure 20: Block diagram of the analog signal processing testchip.

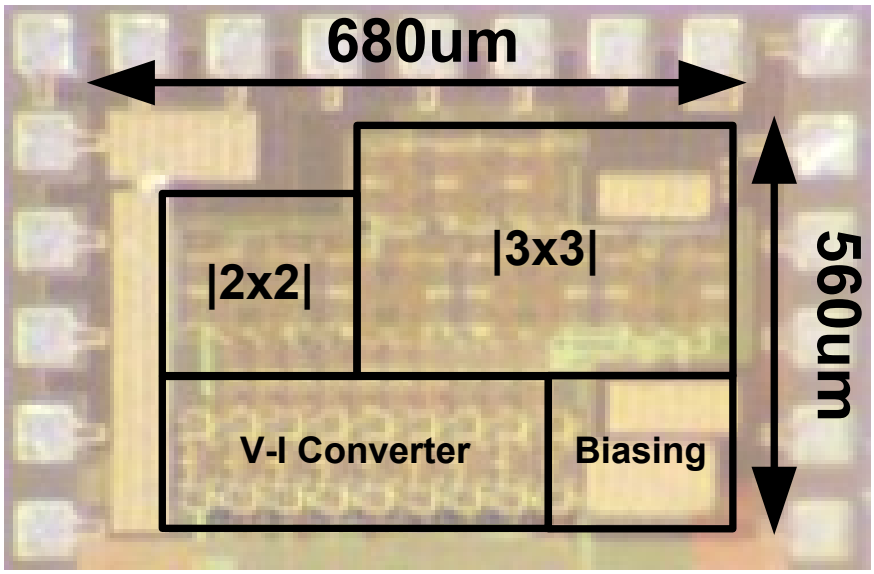


Figure 21: Micrograph of the analog signal processing test chip.

modulation indexes in (11) are swept and the precision is measured. For the 3-by-3 case, b_{13} is swept while the absolute value of all the other indexes, β, are swept independently ($\beta = |b_{ij}|$, where $2 \leq i \leq 3, 1 \leq j \leq 2$). In this way, the precision tendency over the full modulation range can be inferred. In Fiure 22 and Figure 23, the determinants from the measurements and the calculations are compared and the minimum accuracy is plotted together. In the 2-by-2 system, the channel length modulation degrades the precision at the larger output values. On the other hand, in the 3-by-3 system, the mismatches between the 2-by-2 cells and the multiplier cells in Figure 18 introduce additional errors when the output values are low. The precisions of the 2-by-2 and the 3-by-3 systems are above 91 % and 87 %, respectively as shown in Figure 22 and Figure 23.

The maximum data rate is determined by the bandwidth of the system when the input swings are low. as well as the input data. The system bandwidth is ultimately determined by the V-I convertors. With the large input swings, the output signals become slew-limited by the current drivability. To consider both the bandwidth and slew rate, the largest input transitions, $I_B(1 \pm 0.5)$, are applied at various frequencies. Up to 3 kHz rate, the expected results are obtained as in Figure 24 and Figure 25.

The entire system consumes 110.05 μW, where 3.7 μW is used by the 2-by-2 determinant cell, 16.5 μW by the 3-by-3 determinant cell, and rest of the power is used by biasing and the V-I convertors and this implies that the system requires 0.67 nJ per a 2-by-2 determinant computation and 5.5 nJ per a 3-by-3 determinant computation.

3.3.4 Conclusion

In this section, the determinant computing analog signal processing block is presented as an example of an energy-efficient analog signal processing system. By analyzing the subthreshold current mismatches as well as introducing the differential cascode

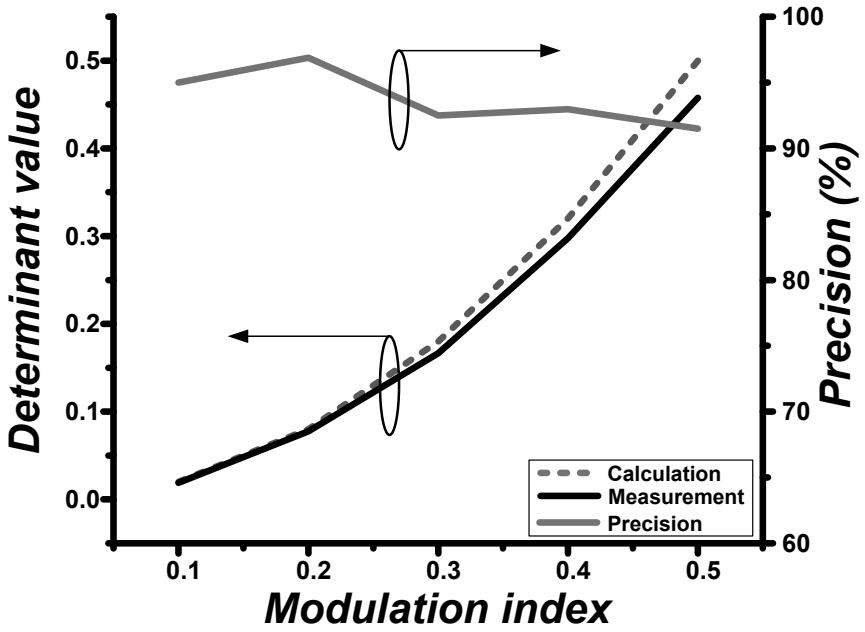


Figure 22: Simulated and measured precisions of the 2-by-2 determinant cell.

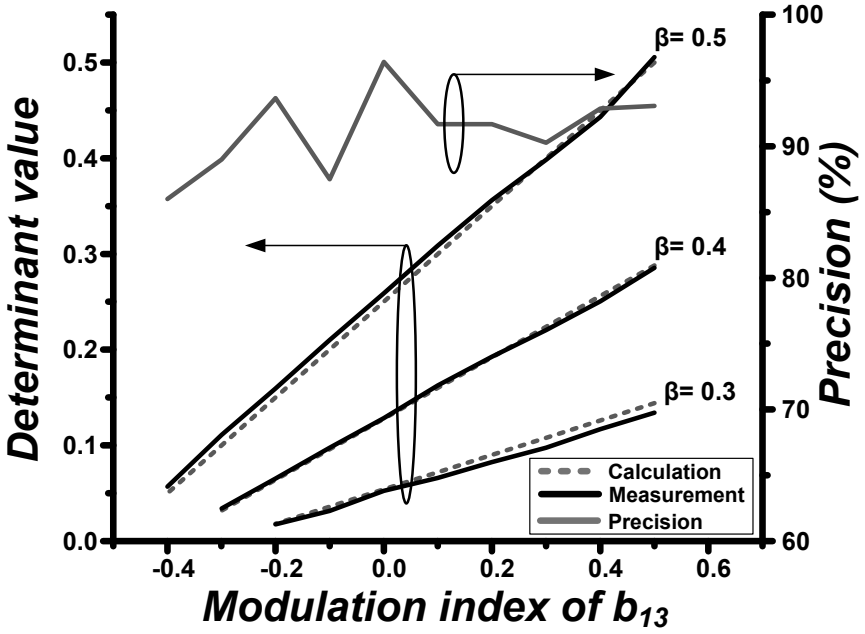


Figure 23: Simulated and measured precisions of the 3-by-3 determinant cell.

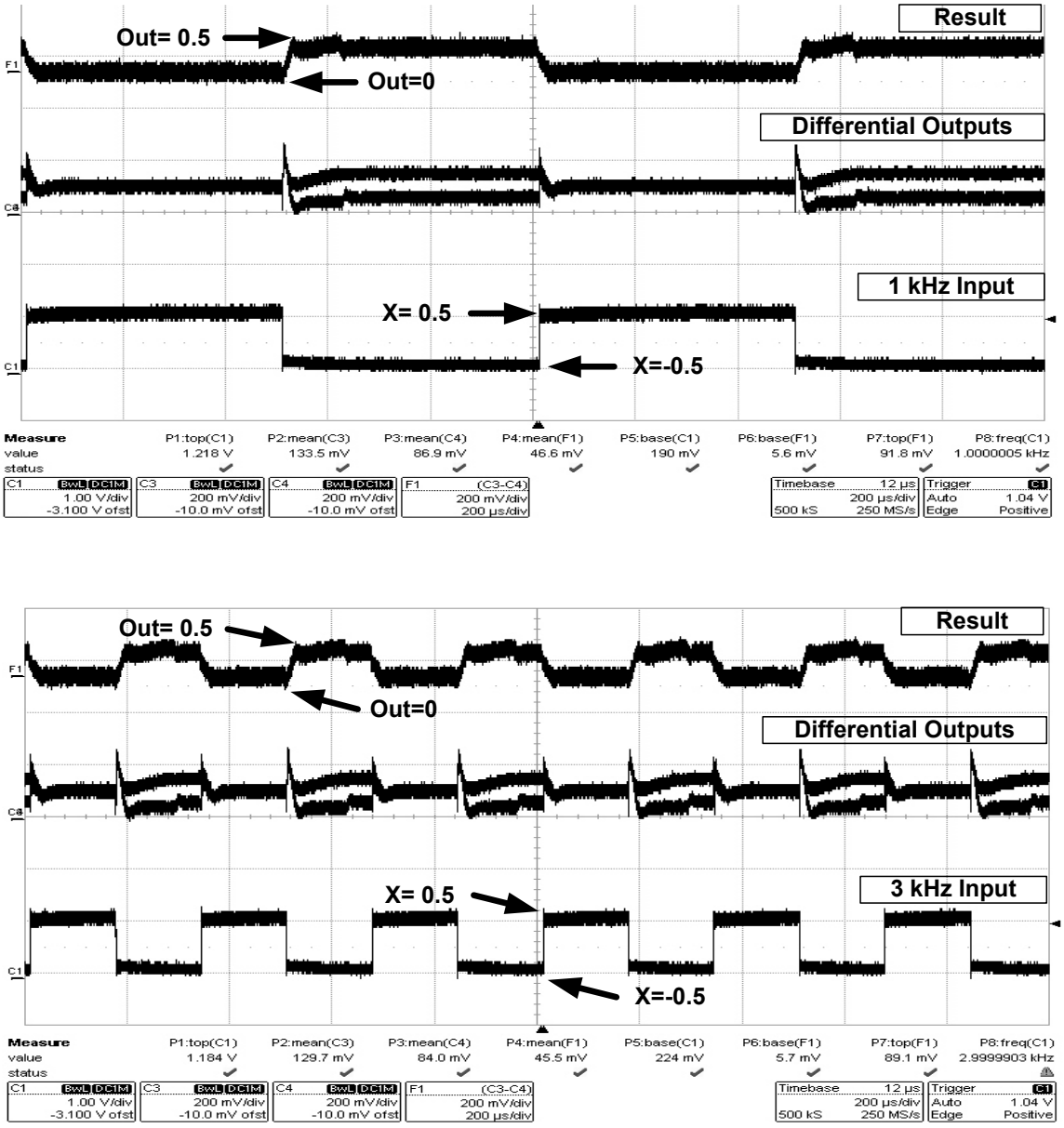


Figure 24: Transient measured waveforms of the 2-by-2 determinant cell when the inputs of 1 kHz and 3 kHz are applied.

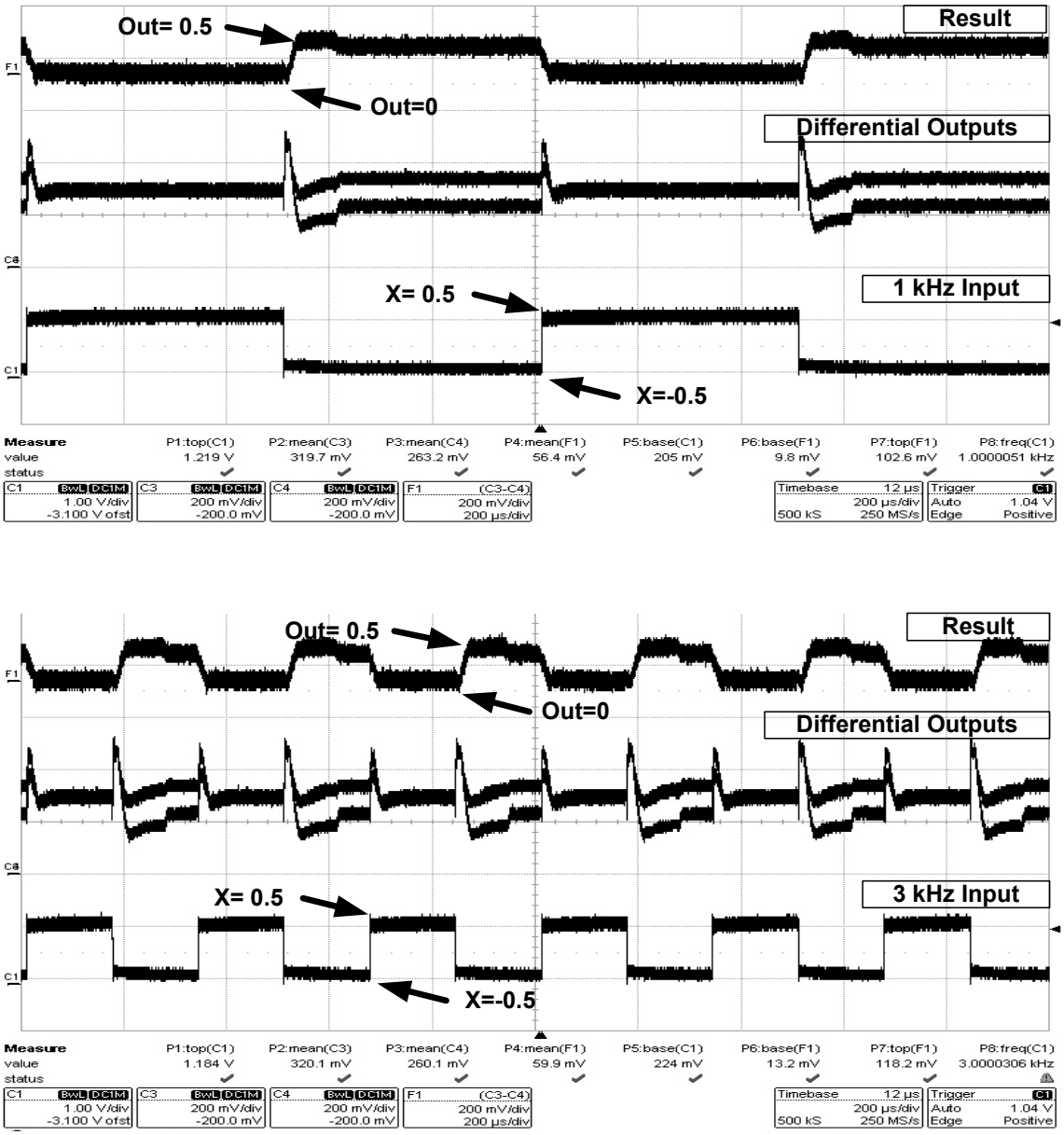


Figure 25: Transient measured waveforms of the 3-by-3 determinant cell when the inputs of 1 kHz and 3 kHz are applied.

Table 1: Performance summary of the subthreshold analog signal processing test chip.

Technology	**TSMC CMOS 0.18 μm**
Active Area	**500 μm x 800 μm**
Maximum Data Rate	**3 kHz**
Energy per Computation	**0.67 nJ (2-by-2)** **5.5 nJ (3-by-3)**
Accuracy	**91 %** **84 %**

architecture, the errors induced from the current variations could be successfully suppressed. This system shows possibility that the analog signal processing can replace the complex and power-hungry digital signal processing in energy-constraint applications.

CHAPTER IV

LOW LEAKAGE CMOS MEMORY UNIT FOR WIRELESS SENSOR NODES

To support an extended period of operational time, a large volume of storage is required as much as improvements in system operating efficiency. With technology scaling, a static-random-access-memory (SRAM) can enjoy considerable advantages in terms of CMOS compatibility, storage density, and implementation costs.

4.1 SRAM Cell

Figure 26 shows the schmatic of a 6-transistor SRAM cell (6T-SRAM). $P1$, $N1$, $P2$, and $N2$ form a positive-feedback latch. As the latch can have two distinguishable states, it can hold either '0' or '1'. $N3$ and $N4$ provide 'access' to the latch; they are often called access transistors. To write or read from the latch, the memory control unit has to open up the access transistors by raising the wordline, WL.

First, to read the datum from the latch, the bitline, the bitlince capacitive loads at BL, and the complementary bitline, $/BL$, are precharged to VDD. Assuming $Q =' 1'$ and $/Q =' 0'$, after the access transistors open up, BL stay at VDD while $N2$ discharges the $/BL$ node. The discharge process can be expedited by increasing the size of the access transistors. However, the strength of the access transistors should not be larger than that of $N1$ and $N2$. Otherwise, during the discharge process, one of the internal latch outputs, $/Q$ in this example, might raise above the trip voltage of the latch. Therefore, to ensure a safe read operation, the size ratio of the access transistors to $N1$ and $N2$ has to be carefully chosen. Due to this sizing restriction, the bitline voltage difference, ΔV_{BL}, changes slowly. Therefore, a sense

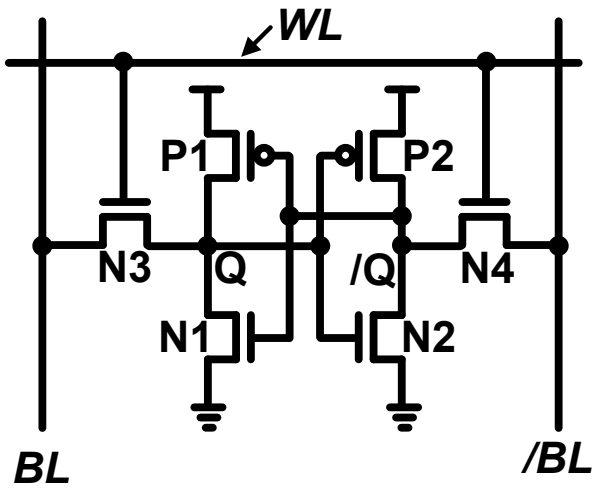


Figure 26: Diagram of a 6T-SRAM cell.

amplifier (SA) is generally attached to expedite the read operation.

To store a desired value to the latch, the desired values are forced onto the latch through the access transistors. Let's assume the latch stores $Q =' 1'$ and $/Q =' 0'$, and we want to store $Q =' 0'$ and $/Q =' 1'$. After the access transistors open up, the write controller try to force $BL = 0$ and $/BL = VDD$. For the read operation to work, $N1$ and $N2$ have to be stronger than $N3$ and $N4$. Therefore, the only way to write $Q =' 0'$ and $/Q =' 1'$ on the latch is the dischage path through $N3$ and $N1$. In other words, the write operation is also a discharge process as the read operation.

4.2 Leakage Issues in Static-Random-Access-Memory Cell

As we migrate to deep-submicron technology for the scaling benefits, subthreshold leakage currents become comparable to active currents as previously shown in Figure 9. The increased leakage currents degrade reliable read/write operations [9][46]. Figure 27 shows the block diagram of a column of 6T-SRAM bit cell array that can have the worst leakage current condition; the active memory cell, the top cell, stores the opposite datum from the rest of the memory cells. Without any leakage currents, when the wordline, WL of the top cell is pulled high after precharging BL

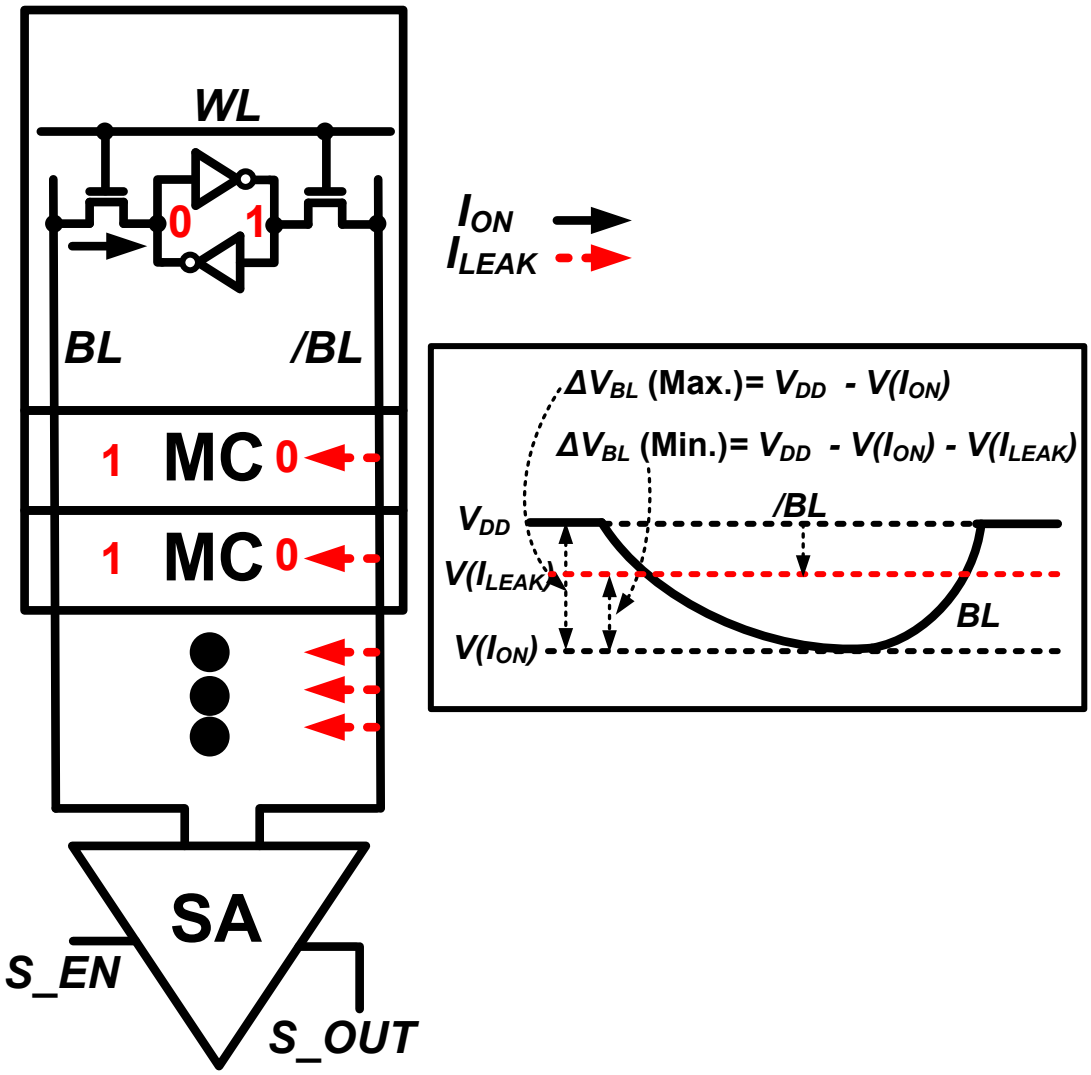


Figure 27: Diagram of a 6T-SRAM bit cell array and conceptual voltage waveforms of BL and BLb showing the leakage current effects.

and $/BL$, $/BL$ stays at VDD, and BL is discharged by the active on-current, I_{ON}. With the leakage currents, I_{LEAK}, represented by the red dotted arrows, after WL is pulled high, the bitline capacitance at $/BL$ is inadvertently discharged by I_{LEAK}. The total amount of the leakage currents from the in-active cells is data-dependent. As the number of the opposing cells increases, ΔV_{BL} decreases. If ΔV_{BL} reaches the minimum voltage difference, $\Delta V_{BL}(SA)$, that should be guaranteed by SA, SA might result in "false read". If the leakage currents increase even further to flip the trip voltage of the inverter latch, the stored datum in the active cell is destroyed.

The insufficient ΔV_{BL} issue due to the leakage currents limit the total number of memory cells that can be stacked in a single column. In addition, the sense amplifier operation speed has to be delayed for robust read outputs. To tackle this issue, the data-dependent leakage currents, I_{OFF}, from the in-active cells was investigated in [7].

4.3 Differential Cell Structures

To mitigate adverse effects from I_{OFF}, a single-ended eight-transitor (SE-8T) cell was investigated. In the SE-8T, the read path is separated from the write path. At the cost of two additional transistors compare to the 6T, the read access transistor and the write access transistor can be sized in favor of each respective operation.

However, the single-ended cell architecture requires a single-ended sense amplifier, which requires longer bit evaluation time and more susceptible to ambient noise than the differential latch-type sense amplifier topology. If a sense amplifier spends more time for the bit evaluation, increase in dynamic power consumption is inevitable. In addition, wireless sensors are operated with low supply voltages and in noisy environments, differential memory cell is preferred.

Figure 28 shows the schmatics of differential SRAM cells: 6T, eight-transistor-leakage-compensating cell (8T-LC), ten-transistor cell (10T).

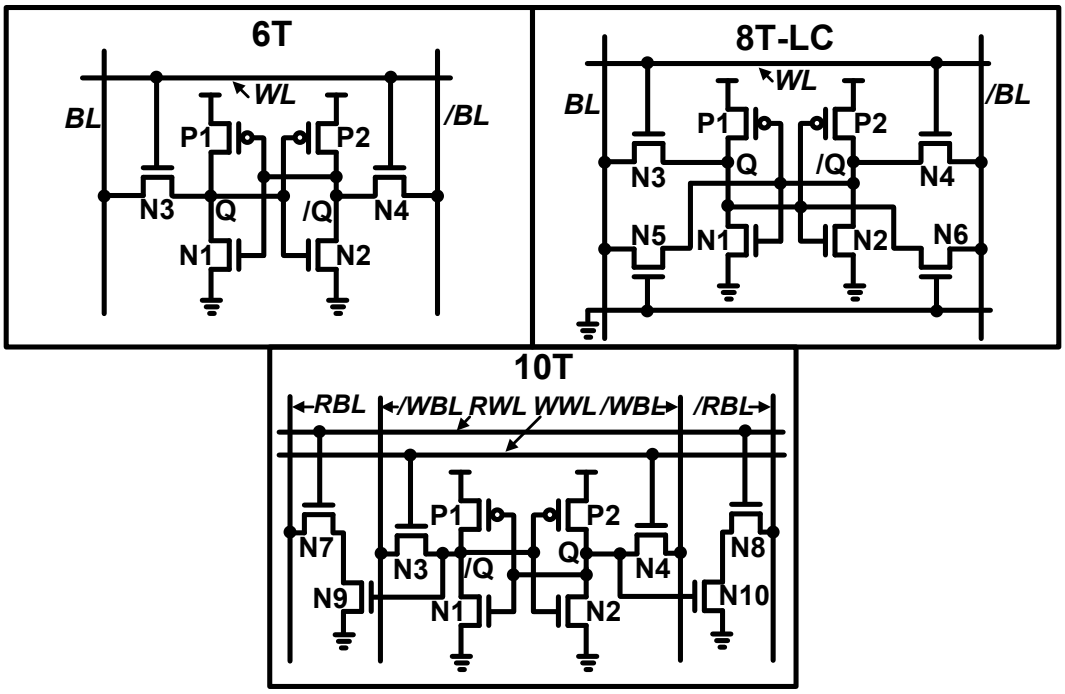


Figure 28: Schematics of differential SRAM cells, 6T, 8T-LC, and 10T.

The 6T has the minimum number of transistors per cell. Howver, it does not have any devcies to fight with the leakage problems.

The 8T-LC looks quite promising in terms of handling the leakage currents [3]. By adding two additional transistors that intentionally generate compensating leakage currents, the overall leakage currents become data-independent. However, because we are intentionally creating additional leakage currents, this cell has higher active power consumption.

The 10T cell uses four more transistors compare to the 6T [32][39]. By dedicating four transistors for the read operation, the read path and the write path can be differentially isolated. In particular, since the read path is not directly connected to the core inverter latch, leakage problems can be alleviated. In other workds,the 10T can offer more reliable SRAM operation at the cost of additional transistors. However, the amount of average leakage currents increase as parasitic leakage current paths are formed by the additional transistors.

4.4 Fully-Gated Ground 10T-SRAM

The problems with the leakage currents generated in inactive memory cells are twofold. First, the leakage currents are directly related to standby power consumption. As wireless sensor devices are inactive for most of the time, slight increase in standby power consumption has devastating consequences on the energy conservation; all of the functional blocks in wireless sensor devices should be focused to preserve as much energy as possible. Another downside is that the leakage currents hamper the reliable operation. In other words, changes in ΔV_{BL} due to the leakage currents are predominantly data-dependent. Therefore, the worst case leakage condition should be considered unless the data dependency is resolved.

To conform to the high capacity and the low leakage-power requirements under the leakage issues, a novel 10T-SRAM employing a fully-gated grounding scheme is proposed (10T-RGND) [42]. The schematic of the 10T-RGND is shown in Figure 29. Since the proposed cell has a read-disturb-free operation as the SE 8T-SRAM, memory failures due to the leakage current coupling can be well-controlled. In addition, the ground node of the read port is only grounded when the cell is being accessed to reduce the leakage currents.

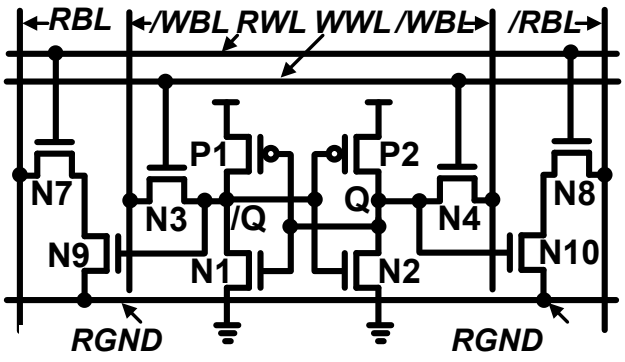


Figure 29: Schematic of the 10T-RGND.

4.4.1 Operation

In the proposed cell, the source nodes of the bottom pass transistors are selectively grounded by a row decoder only when the memory cell is accessed. In the meanwhile, those of inactive memory cells are forced to a supply voltage as shown in Figure 30. By adaptively changing the source potentials, leakage currents originated from inactive memory cells are reduced substantially.

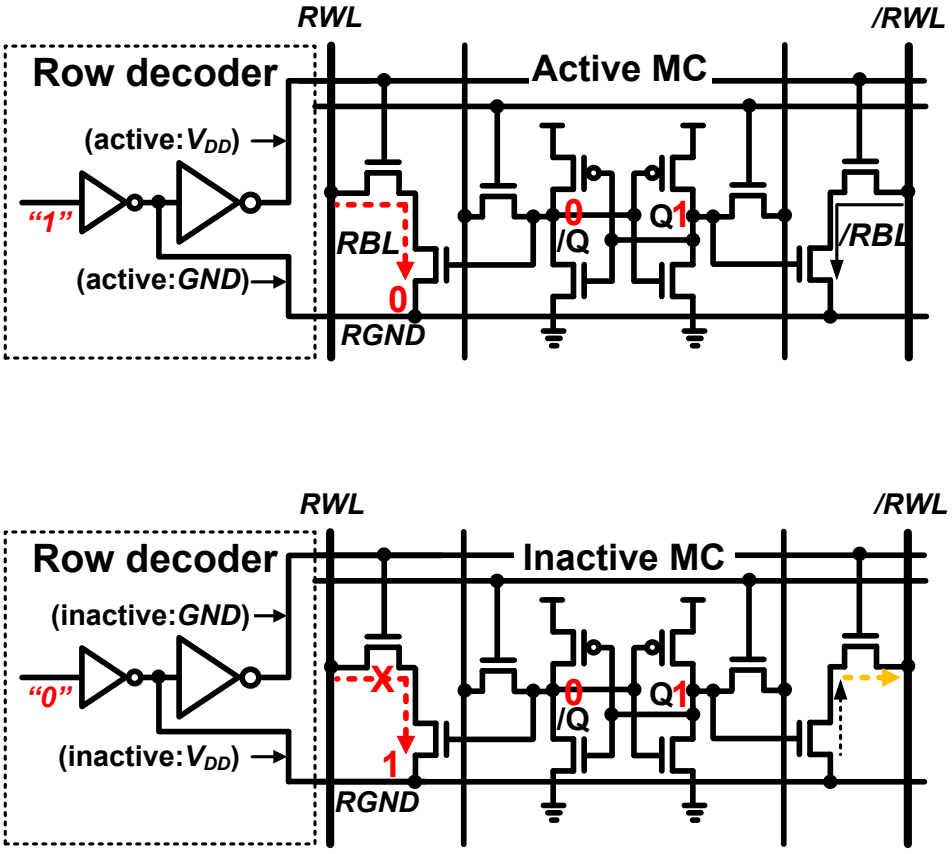


Figure 30: Diagrams of the 10T-RGND cell when it is active (top) and inactive (bottom).

4.4.2 Simulation Results

The leakage-compensating 8T-LC [3] and the 10T [32] were proposed to deal with the leakage issues. Unlike the SE-8T, the 8T-LC does not have separate read/write ports. Instead, the two extra transistors ($N5$ and $N6$ in the 8T-LC in Figure 31) intentionally

create leakage currents that cancel out data-dependent leakage mismatches. However, the additional compensating currents will increase static power consumption. At the cost of additional two more transistors, the 10T achieves differential operation so that it can be faster and more reliable than the SE-8T. However, the 10T still suffers from data-dependent leakage mismatches. The corresponding schematics and layouts of a 6T, an 8T-LC, and a 10T-RGND are shown in Figure 31.

To evaluate leakage current effects on each cell, a test structure is configured in a 45nm CMOS SOI process as shown in Figure 32. The active cell holds "1" ($BL = VDD$ and $/BL = GND$). The total number of inactive cells is N while the number of opposing cells ($BL = GND$ and $/BL = VDD$) is M. The data-dependent leakage mismatches of 6T, 8T-LC, 10T, and 10T-RGND can be estimated as (15) - (18).

$$\begin{aligned} \Delta I_{6T}(M) &= I_{ON-6T} - M \times I_{OFF-6T} \\ &\leq I_{ON-6T} - N \times I_{OFF-6T} \end{aligned} \tag{15}$$

$$\begin{aligned} \Delta I_{8T-LC}(M) &= I_{ON_8T-LC} - M \times I_{OFF-8T-LC} + M \times I_{OFF-8T-LC} \\ &= I_{ON-8T-LC} \end{aligned} \tag{16}$$

$$\begin{aligned} \Delta I_{10T}(M) &= I_{ON-10T} - M \times I_{OFF-10T} \\ &\leq I_{ON-10T} - N \times I_{OFF-10T} \end{aligned} \tag{17}$$

$$\begin{aligned} \Delta I_{10T-RGND}(M) &= I_{ON-10T-RGND} - M \times I_{OFF\_0T-RGND} \\ &\leq I_{ON-10T-RGND} - N \times I_{OFF_10T-RGND} \end{aligned} \tag{18}$$

The leakage effects on the bitline voltages (BL and $/BL$) were simulated as the number of opposing cells is increased. The test structures in Figure 32 were used, and

the worst leakage condition was applied - $VDD = 1.0\,\mathrm{V}$, temperature = 125 degree celsius, and the fast corner process. When a bit evaluation period of 200 ps was applied, the maximum numbers of opposing cells that can be handled by the 6T and the 10T were 230 and 320 respectively. Meanwhile, the 8T-LC and the 10T-RGND could handle beyond 1024 number of opposing cells as shown in Figure 33.

The static leakage currents and ΔV_{BL}'s of the 6T, the 8T-LC, the 10T, and the 10T-RGND test structures are plotted in Figure 34. When 1024 bits of each cell are stacked, the static leakage currents of the 6T, the 8T-LC, the 10T, and the 10T-RGND are 1900 μA 2460 μA, 2790 μA, and 2330 μA, respectively. In terms of the leakage power consumption alone, the 6T structure seems to be the most power efficient solution. However, if we assume ΔV_{BL} of 50 mV is required to overcome sense amplifier offsets, the numbers of allowed bits in a single column turn out to be 80, 230, 574, and 810 for the 6T, the 8T-LC, the 10T, and the 10T-RGND, respectively. Meanwhile, V_{BL} and $V_{/BL}$ of the 8T-LC decrease more abruptly as the number of the opposing cells increases than those of the 10T-RGND. These results indicate that the swing range of BL and $/BL$ (V_{SWING}) of the 8T-LC is larger than that of the 10T-RGND consuming more dynamic power. V_{SWING} of the 6T, the 8T-LC, the 10T, and the 10T-RGND with 1024 opposing cells are 286 mV, 503 mV, 385 mV, and 118 mV, respectively. The small V_{SWING} of the 10T-RGND can compensate the redundant power consumption for driving the $RGND$ line on every clock cycle.

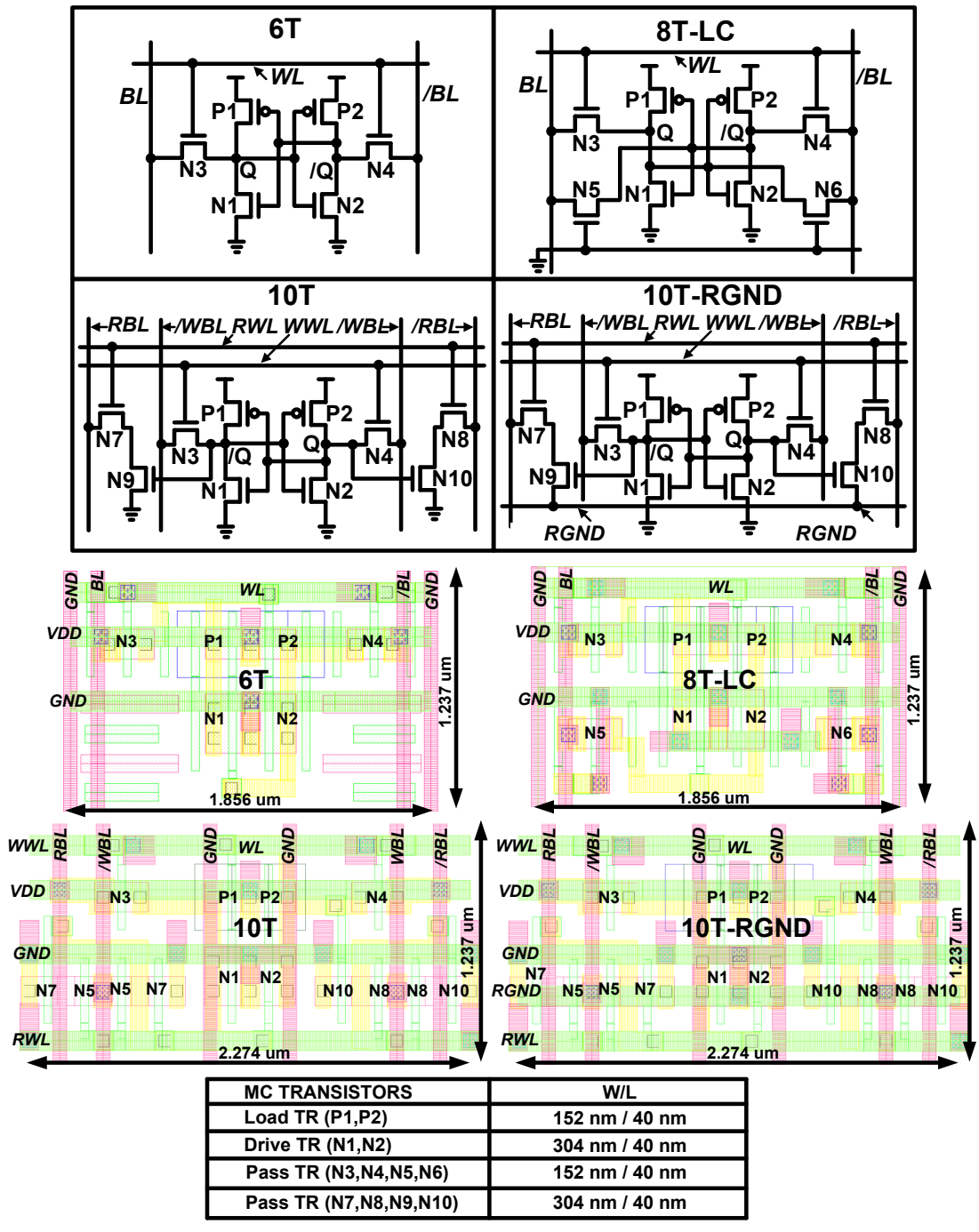
The figure of merits (FOM) of the tested cells can be derived by the area (A), the total static leakage current (I_{LEAK}), V_{SWING}, and the number of allowed stackable bits (NoB) at $\Delta V_{BL} = 50\,\mathrm{mV}$ as in (19).

$$FOM = \frac{NoB}{A \times I_{LEAK} \times V_{SWING}} \tag{19}$$

FOM's are calculated by simulation a 0.06, 0.2, 0.08, and 1.04 for the 6T, 8T-LC, 10T, and 10T-RGND, repectively.

4.4.3 Conclusion

As the leakage currents affect ΔV_{BL} more aggressively as we migrate further into deep submicron technology, resolving the leakage issue is crucial for robust SRAM operations. In this section, the 10T-RGND is proposed to limit the leakage currents dynamically. While the 10T-RGND occupies larger area due to the additional four transistors than the 6T, the simulation shows that the 10T-RGND has less V_{SWING}, and larger NoB at $\Delta V_{BL} = 50\,\text{mV}$ than the 6T, the 8T-LC, the 10T. The FOM of the 10T-RGND is larger than 6T, 8T-LC, and 10T by 17x 5.2x, and 13x, respectively, which indicate that 10T-RGND can be among the best candidates for the differential-sensing MCs in deep submircon technology.



MC TRANSISTORS	W/L
Load TR (P1,P2)	152 nm / 40 nm
Drive TR (N1,N2)	304 nm / 40 nm
Pass TR (N3,N4,N5,N6)	152 nm / 40 nm
Pass TR (N7,N8,N9,N10)	304 nm / 40 nm

Figure 31: Schematics and layouts of a 6T, an 8T-LC, and a 10T-RGND.

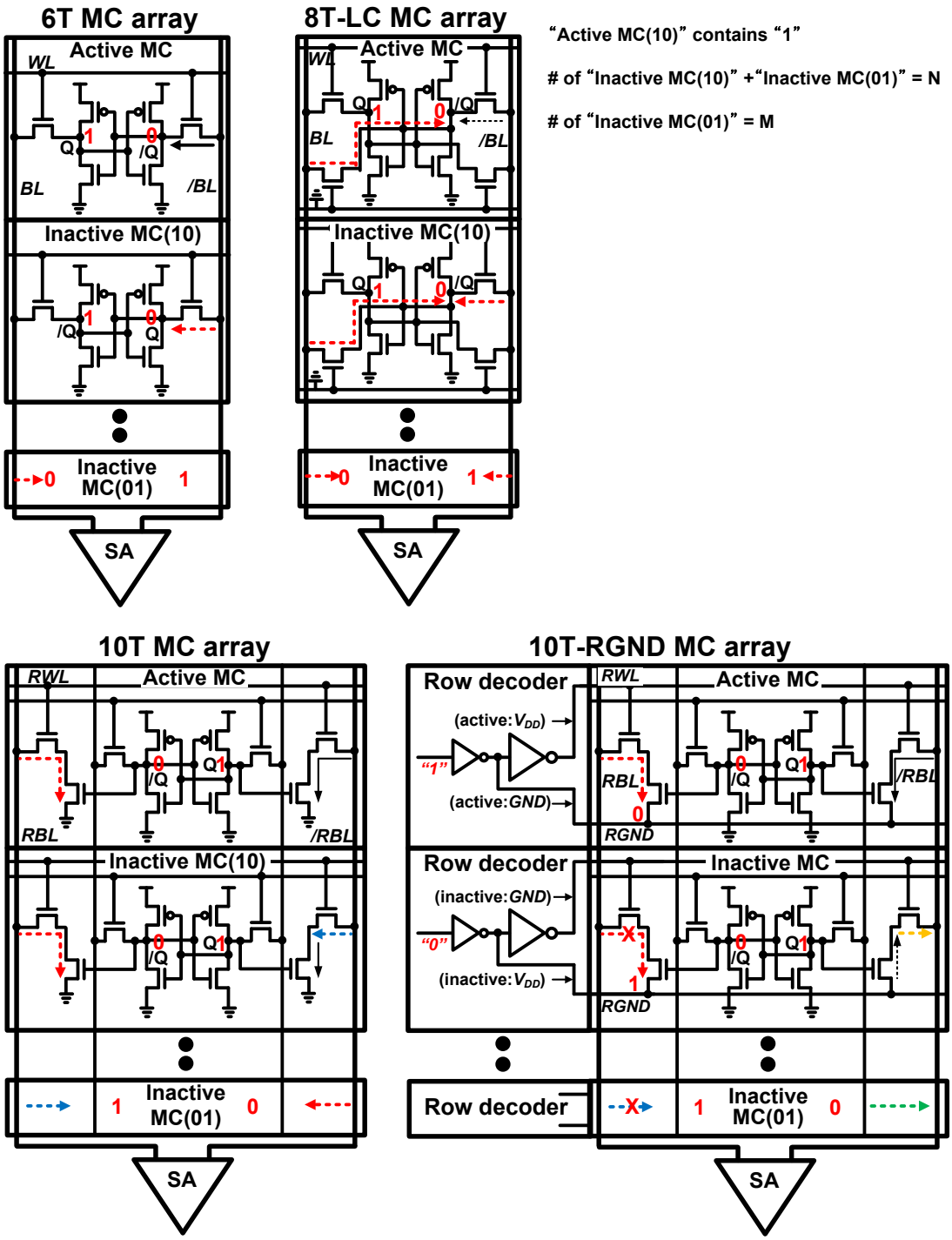


Figure 32: Test structures of 6T, 8T-LC, and 10T-RGND to evaluate the effects of data-dependent leakage currents.

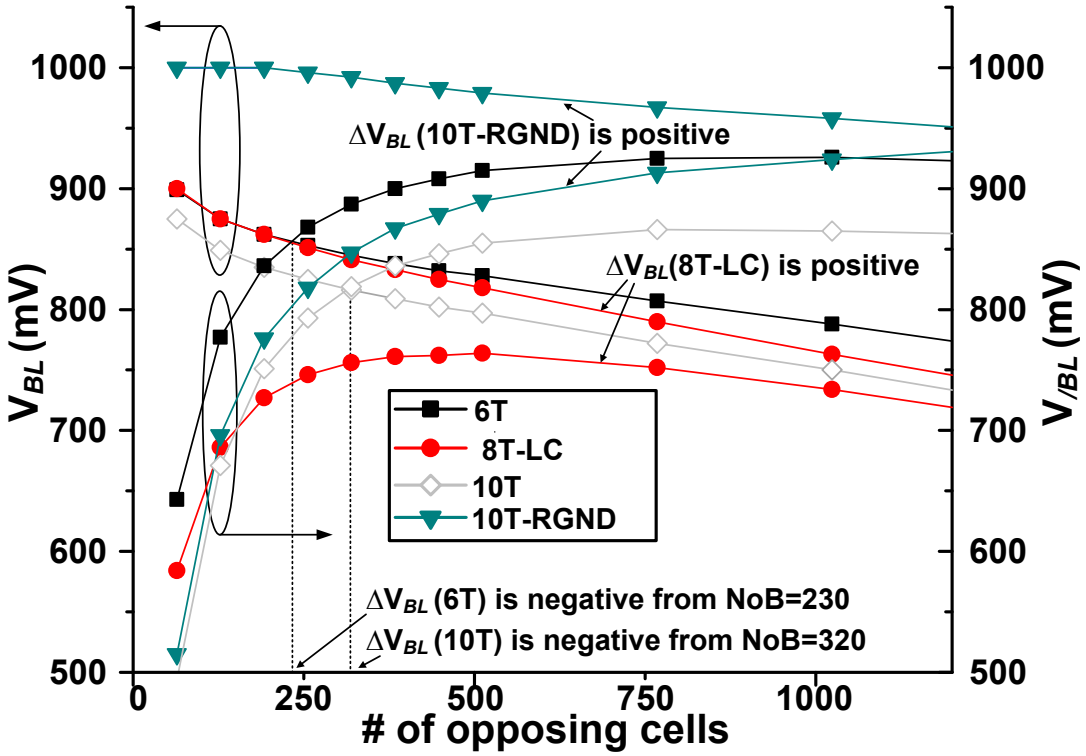


Figure 33: V_{BL} and $V_{/BL}$ of 6T, 8T-LC, 10T, and 10T-RGND versus the number of opposing cells.

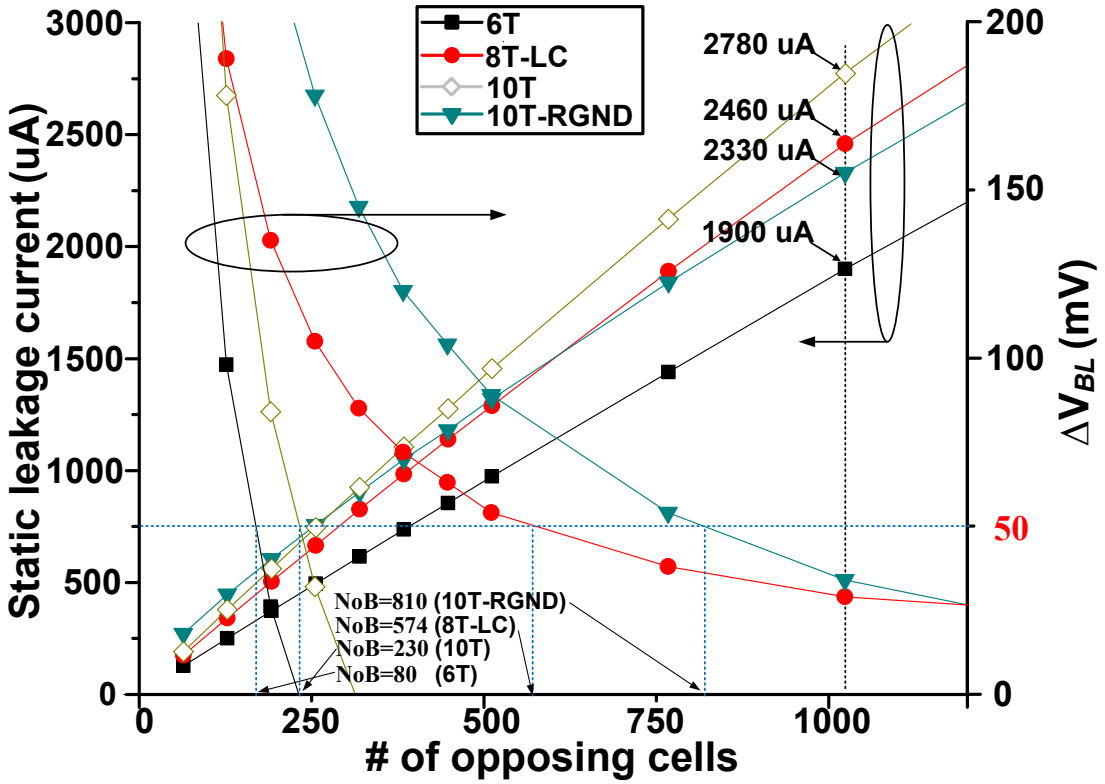


Figure 34: Static leakage currents and ΔV_{BL}'s of 6T, 8T-LC, 10T, and 10T-RGND versus the number of memory cells.

CHAPTER V

CMOS RECTIFIER FOR WIRELESS POWER TRANSMISSION

5.1 Possible Energy Sources for Wireless Sensor Devices

Figure 35 shows the Ragone chart, where power density and energy density for different kinds of energy sources are compared [47]. The y-axis represents the total amount of energy per unit mass, m, in a energy source, or energy density as in (20), and the x-axis represent the rate of the stored energy that can be delivered per unit mass, or power density as in (21).

$$EnergyDensity = \frac{V \times I \times t}{m} \tag{20}$$

$$PowerDensity = \frac{V \times I}{m} \tag{21}$$

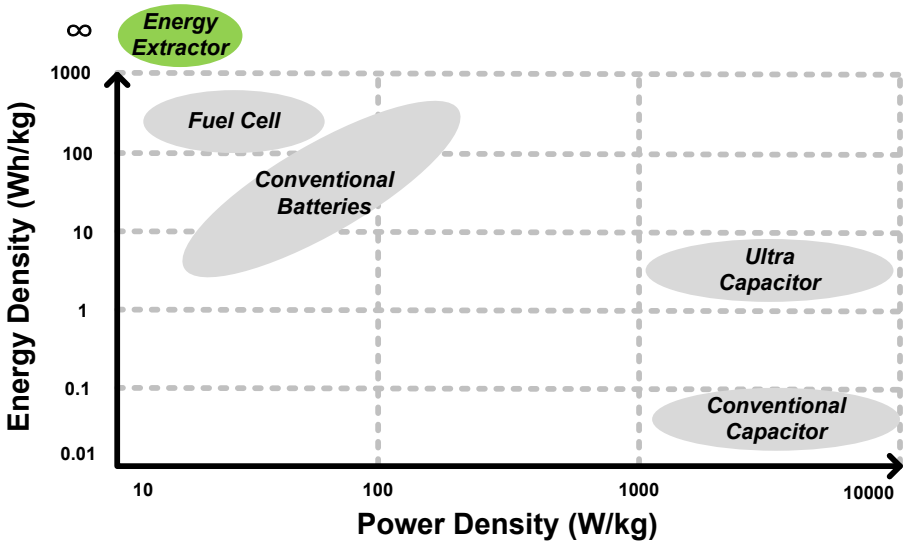


Figure 35: Ragone chart.

Table 2: Energy extractor comparison.

Type	Attributes	Challenges
Solar	Photovoltaic cells. Widely used.	Heavily dependent on light conditions.
Thermal	Thermoelectric generators. Bi-directional usage.	Heat sinks required.
Vibrational	Piezoelectric devices. Bi-directional usage.	Mechanical resonator required.
Electromagnetic	Inductively-coupled links. Energy and data can be transferred.	Dependant on matching conditions.

For conventional capacitors or ultra capacitors, they have fairly high power density, but low energy density. Conventional batteries including li-ion batteries have both reasonable power density as well as energy density. Fuel cell batteries show even higher energy density than conventional batteries but less power density. Unlike, these energy sources which have finite energy density, energy extractors provide virtually infinite energy density, which would be the perfect fit for wireless sensor applications.

There are four different energy extractor types that can be applied to wireless sensor applications. The solar type utilizes photovoltaic cells to harvest solar energy. The solar harvesting is widely used in both low-power and high-power applications. However, the harvesting performance is heavily dependent on ambient light conditions. The thermal type utilizes thermoelectric generators to harvest the ambient thermal gradient. Thermoelectric generators can convert the ambient thermal gradient into electrical energy, and they can also function as an electric cooler if external energy is applied. The thermoelectric generator requires temperature difference for the energy conversion. Therefore, a well-designed heat sink is essential for high energy conversion efficiency. The vibrational type utilizes piezoelectric devices to extract vibrational energy. Just like thermoelectric material, piezoelectric devices can be bi-directional;

energy can be exchanged for vibrational motions. However, ambient vibrational motions contain random frequency components, and piezoelectric devices have their own natural resonant frequency. Thus, the vibrational type requires mechanical resonators for practical applications.

The electromagnetic type often uses inductively-coupled links; although far-field energy extraction can be used, the extractable energy level in far-field decays substantially as the communication distance increases, and the far field data transmission from the receiver side would put too much burden on the system energy budget. Inductively-coupled links transform time-varying magnetic flux into AC currents. The performance of this type is affected by the frequency matching conditions. The main difference between the electromagnetic type to the rest is that the electromagnetic type does not harvest ambient energy. Wireless energy must come from a base station, which is also responsible for data communication. The fact that energy and data can be transferred through an inductive link makes the electromagnetic type a good candidate for wireless sensor applications.

5.2 Inductively-Coupled Link

For wireless sensor devices, wireless power transmission has been a popular solution because it provides a more reliable energy source than energy scavenging schemes [5]. A conventional remotely powered system is described in Figure 5. The inductive link (or an antenna) catches the electromagnetic energy generated by the base station. The rectifier then converts AC energy into DC energy, which is used in the following processing blocks.

However, the maximum transmitted power level at the base station should be restricted due to human safety issues. Therefore, given the path loss and the matching loss, the voltage conversion efficiency ultimately determines the total available DC energy.

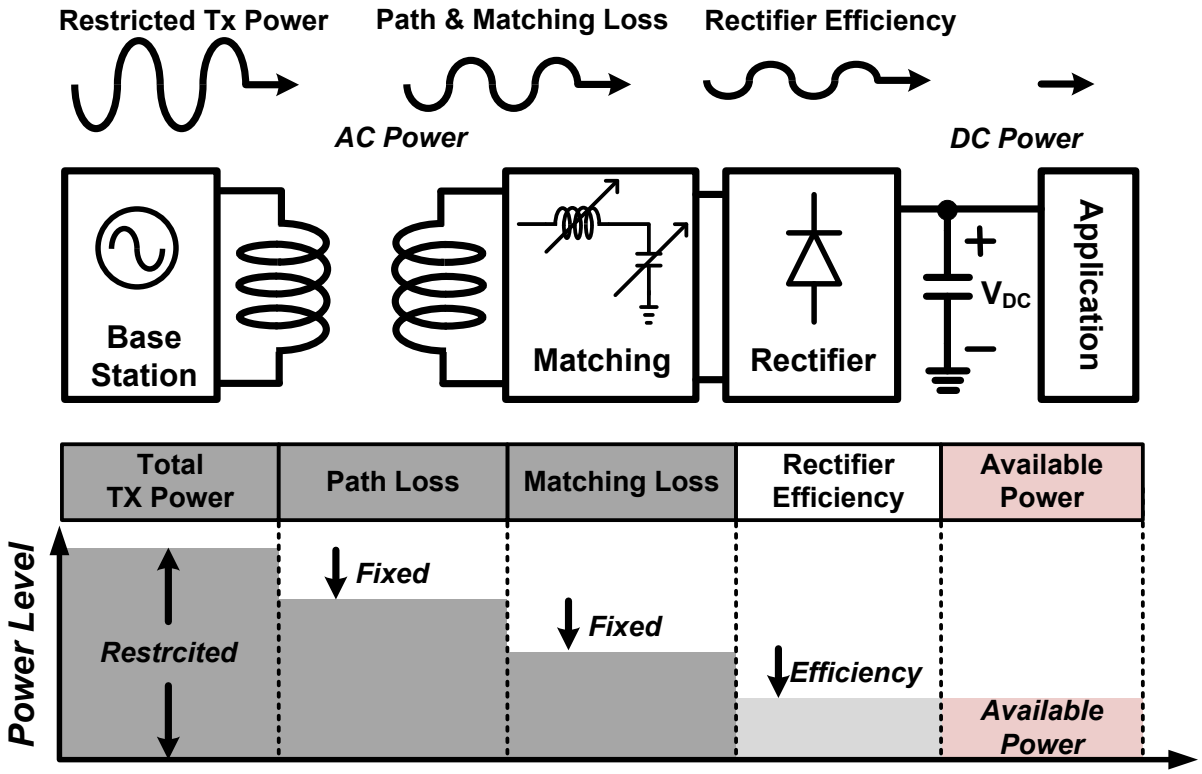


Figure 36: Diagram of a typical remotely powered system.

5.3 Rectifiers in High-Power and Low-Power Applications

Rectifiers are widely used in high-power applications whose power levels are from watts to mega watts and low-power applications whose power levels are from micro watts to watts. High power rectifiers can be categorized into output controllable rectifier, or line-frequency phase-controlled converters, and free-running rectifier, or line-frequency diode rectifiers. The line-frequency rectifiers can control the amount of AC-to-DC conversion period by using thyristors, whose conduction condition can be controlled by external current pulses. If thyristors form a full-bridge converter, either a single phase or a three-phase, the current direction can be bi-directional depending on the thyristor conduction timing. The line-frequency phase controlled converters are used in high-voltage DC power transmission and motor drives with regenerative capabilities. On the other hand, the line-frequency diode rectifiers utilize high voltage diodes whose conduction condition only depends on the input voltage. Therefore, the

Table 3: High power rectifier and low power rectifier.

Type	High Power	Low Power
Output Controllability	Controllable Uncontrollable	Uncontrollable
Devices	Thyristers High voltage diodes	High-speed diodes Transistors
Applications	High voltage power transmission (Bi-directional) Motor drives	Energy Scavenge
Issues	Line distortion Stable operations	High voltage conversion efficiency

output voltage and power depends on the input signal. As most of the grid power input is in AC, the line-frequency rectifiers provide a cost-efficient solution for DC power converter systems. For the high power rectifiers, the input is coming from an electrical grid, and the distortion in rectifier is regulated.

Low power rectifiers are used for scavenging ambient AC energy, and the input power is usually limited. Therefore, the rectifiers do not try to control the output voltage but to generate the highest possible DC voltage. As the low power applications involve kilo-hertz to mega-hertz input signals, high-speed diodes or transistors are used.

5.4 Semi-Active High-Efficient CMOS Rectifier

There are several ways to implement a low-power rectifier. First of all, there can be a full-wave rectifier and a half-wave rectifier. As the name indicates, the full-wave rectifier pumps twice as much charge as the half-wave one. Thus, the full-wave rectifier topology is chosen. Second, a rectifier can be implemented only with standard CMOS devices while it can be also implemented with schottky diodes or even floating-gate devices. Since the standard CMOS offers better compatibility and it is cheaper, the All-CMOS solution is preferred over the hybrid implementation. Finally, a rectifier

can be either passive or semi-active. The term, semi-active implies that the rectifier consumes some of its own rectified dc-power so that it prevents some negative effects that degrade conversion efficiency. Therefore, the semi-active one is selected.

There are pros and cons in the all-CMOS semi-active full rectifier. First, the full-wave rectifier pumps more charge and All CMOS implementation is cheaper and it offers better compatibility. Finally, in normal condition, it can achieve higher conversion gain.

However, there are some disadvantages. Since it is consuming some of its own rectified power, at certain conditions (such as when either frequency is high or input power is extremely low), the passive solution can be more effective. In such case, implementation with non-standard CMOS devices such as floating gates and schottky diodes might be a better approach.

For high voltage conversion efficiency, a new semi-active high-efficient CMOS rectifier is proposed. The proposed rectifier successfully handles the reverse charge leakage which is the main reason for the conversion efficiency degradation. In addition, an adaptive body bias control technique is adopted to improve reliability. Although the proposed circuit architecture might not be the optimum solution for all of the wireless sensor applications, the proposed design techniques can be selectively applied to a majority part of the applications in which efficiency and reliability improvement and low cost implementation play important roles.

5.4.1 Rectifier Topologies

- Passive Rectifier

A diode-bridged rectifier is a simple way to realize a full wave rectifier. Schottky diodes are often employed to enhance the conversion efficiency. However, considering additional costs and the fact that Schottky diodes are not supported in all

CMOS technologies, a CMOS-based implementation is considered as practical solutions [23][30]. Moreover, the CMOS implementation offers better compatibility with the following processing block which is usually implemented in a CMOS technology.

A CMOS diode-bridged rectifier in Figure 37 (a) picks up differential RF-input during both input transition cycles - positive and negative. The black line represents the positive cycle and the gray line represents the negative cycle. At each cycle, the corresponding complementary diode pair turns on and delivers the input RF current to the output at the expense of $2 \times V_{TH}$ drop. Thus, this configuration inherently suffers from $2 \times V_{TH}$ voltage drop.

One way to improve this threshold voltage drop is to use a cross-coupled PMOS pair shown in Figure 37 (b) [15]. During each cycle, the voltage drop across the cross-coupled PMOS pair (V_{DS}) depends on the input current level and if the input current level is sufficient and the transistors are properly sized, V_{DS} can be lower than the V_{TH}. However, the bottom diodes still suffer from the V_{TH} drop.

If a cross-coupled NMOS pair is adopted instead of the two bottom diodes, the remaining V_{TH} drop issue can be solved as shown in Figure 37 (c) [30]. However, on every cycle, there exists a period where the output node potential is higher than that of the input node. When this happens, the cross coupled pairs cannot be turned off completely, thereby causing charge leakage. The charge leakage then degrades the conversion efficiency. In addition, the rectifier circuit does not have a stable supply voltage that can guarantee the highest potential in the system. Therefore, if PMOS body terminals are statically tied to fixed potentials, the source-body (or drain-body) diodes of PMOS transistors can be forward-biased.

- Active and Semi-Active Rectifier

Existing literatures propose utilization of several active circuitries to enhance the conversion efficiency of rectifiers [23][36][43]. In [43], the V_{TH} cancellation technique

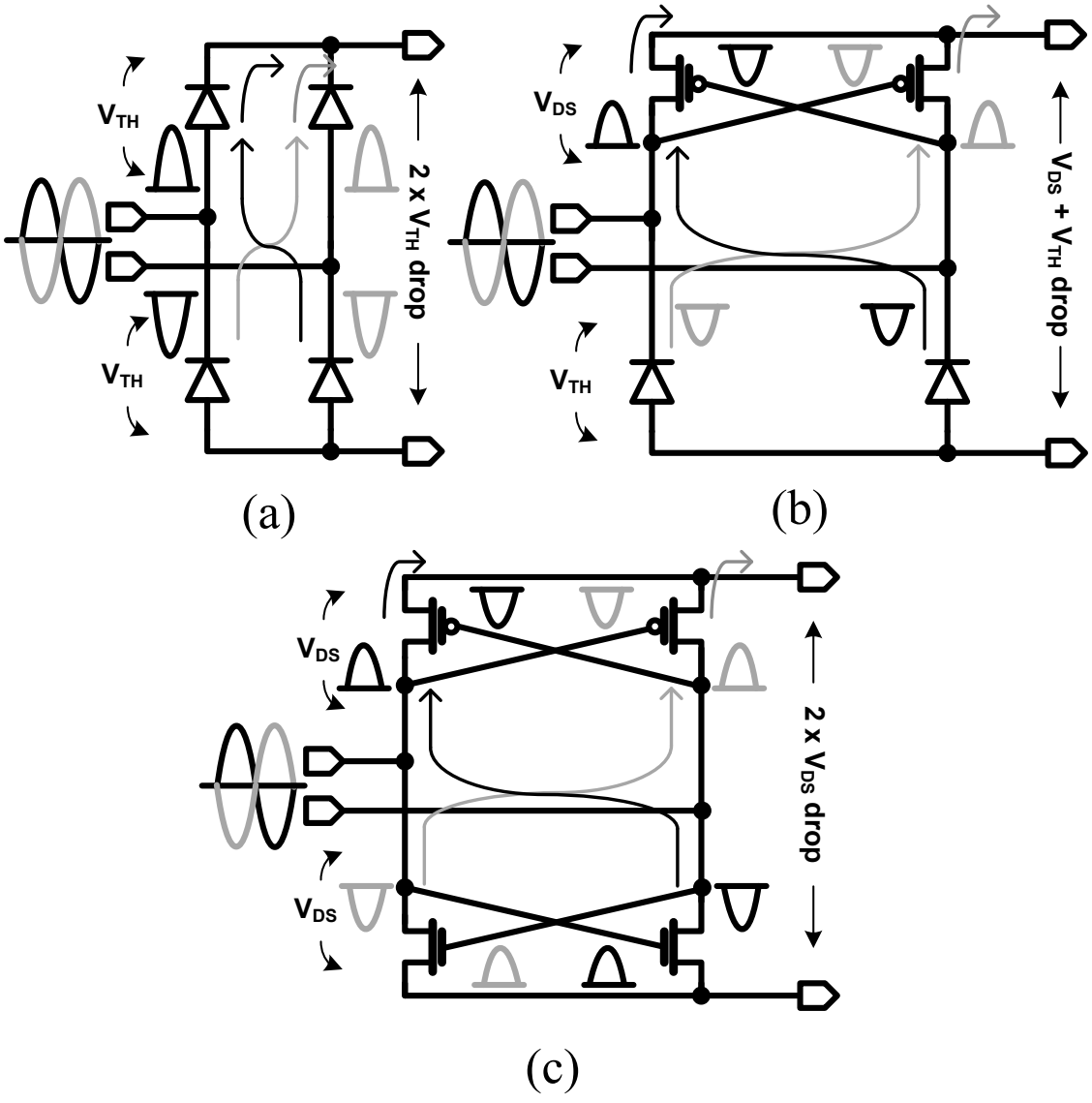


Figure 37: Diagrams of (a) Full-wave rectifier, (b) PMOS cross-coupled rectifier [15], and (c) NP-cross-coupled rectifier [30].

was adopted to lower the threshold voltage drop of diode-connected transistors. However, this approach requires external reference and supply voltages. In [23], an active diode was utilized to reduce conduction drop. The active diode was implemented with a four-input-comparator that does not require external supplies. However, since this comparator does not use an external supply, and it is connected to NMOS transistors, the NMOS transistors cannot be fully turned on. Therefore, if this rectifier cell is multiply stacked to obtain higher voltage conversion gain, the active diodes in the latter stages would suffer from high resistive current paths.

5.4.2 Charge Leakage Analysis

When we think about the operation of a NP-cross coupled rectifier in Figure 38, the transistors can be considered as variable resistors. Depending on the input voltage level, which changes periodically, the resistance is determined. For instance, the first peak of the input voltage waveform, $MP1$ and $MN2$ would have their lowest resistance while $MP2$ and $MN1$ would have their highest. Thus, the current is flowing through $MP1$ and $MN2$.

However, there are some problems that affect conversion efficiency. Since the variable resistors change their values according to the input signal, we do not have a control of the values of the resistors. Thus, as the AC-signal goes through the rectifier, there is always a certain period of time that the output is higher then the input and the resistance is small. Consequently, the current flows from the output to the input. In other words, the reverse charge leakage happens.

To observe this problem, a sinusoidal wave with 1-V amplitude and 1-MHz frequency is applied to the single stage NP-cross-coupled rectifier shown in Figure 38. As the input node, V_{+-}, fluctuates smoothly, the cross-coupled PMOS and NMOS pairs cannot turn on and off abruptly. When the output node is charged up to the targeted

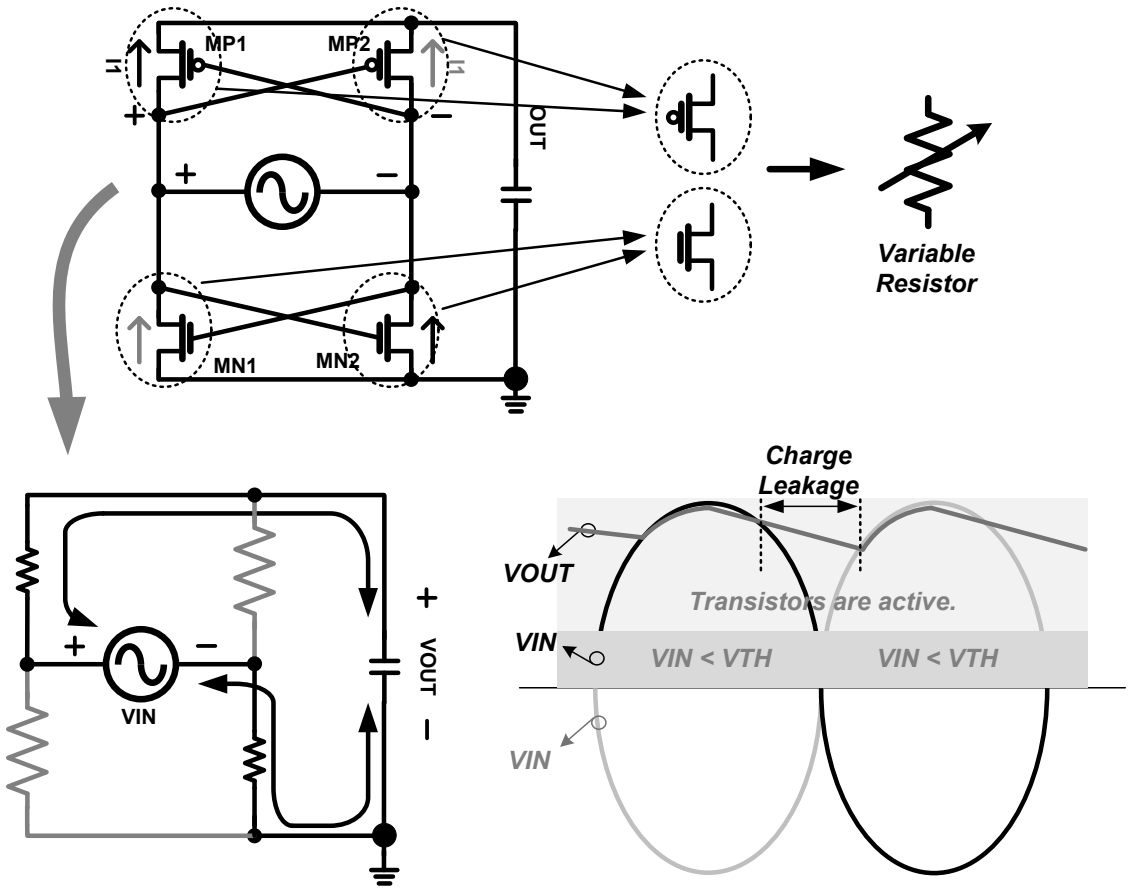


Figure 38: Diagram of a NP-cross coupled rectifier and its charge-leakage problem.

level, the output voltage can be higher than the input voltage for considerable duration of time. Since the PMOS cross-coupled pair cannot be turned-off completely during this period, the charge stored at the load capacitor discharges through the partially turned-on PMOS pair.

The corresponding voltage and current waveforms are shown in Figure 39. The rectifying cycle can be divided into 5 regions. As the chosen topology is a full-wave rectifier, the five regions repeat every half-input period.

- **Region 1 :** The gate drive voltage, V_{+-}, is smaller than V_{TH}, and the output node voltage is lower than the input voltage. Therefore, there is subthreshold conduction which has minor effects on the leakage problem.

- **Region 2 :** The gate drive voltage exceeds V_{TH}. Since the output node,

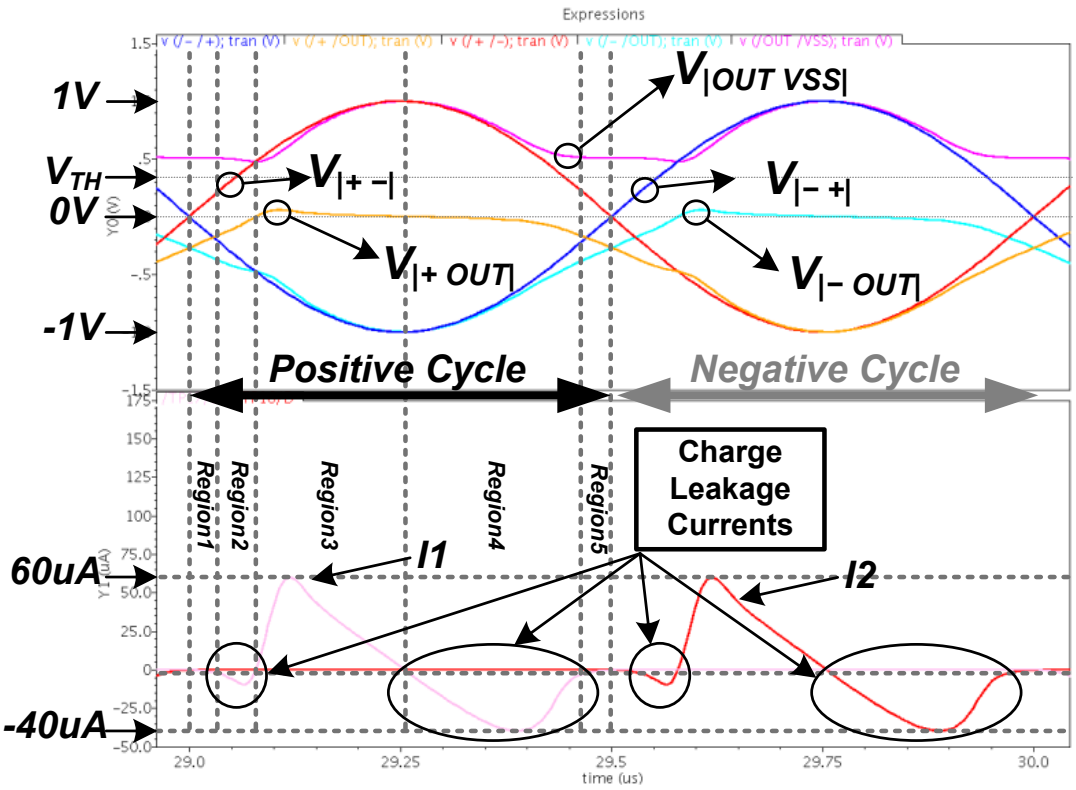


Figure 39: Simulated voltage and current waveforms of the NP-cross coupled rectifier in Figure 38.

V_{OUTVSS}, is still lower than the input voltage, $MP1$ starts conducting current and current flows from output to input.

- **Region 3 :** As the input voltage increases, it becomes larger than the output voltage. When the gate drive voltage is higher than V_{TH}, the output capacitor is charged.

- **Region 4 :** The gate drive voltage is still higher than V_{TH}, but the input voltage is lower than the output node voltage. Thus, the output node is discharged until $MP1$ turns off.

- **Region 5 :** The gate drive becomes smaller than V_{TH}, and there is subthreshold conduction as in Region 2.

5.4.3 Proposed Architecture

The proposed semi-active high-efficient CMOS rectifier cell is shown in Figure **??** (a). It utilizes the NP-cross-coupled rectifier to minimize intrinsic voltage drop. Moreover, the leakage control comparators, shown in Figure **??** (b), are inserted in the PMOS cross-coupled connection to alleviate the reverse leakage problem. In addition, the active body-biasing (ABB) technique is adopted to prevent the PMOS body-junction diodes from turning on for better reliability of the rectifier as shown in Figure **??** (c) [6][40].

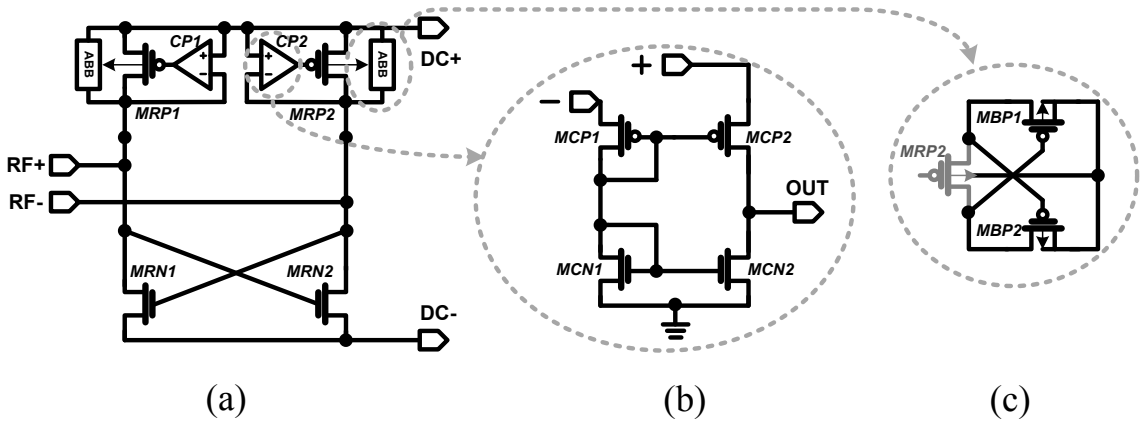


Figure 40: Diagram of (a) the proposed rectifier cell, (b) the leakage control comparator, and (c) the active body biasing block [6][40].

- **Semi-Active Leakage Control Comparator**

For the NP-cross-coupled rectifier, the transistors can be regarded as variable resistors, of which values vary in a non-linear fashion as the operating regime alternates between saturation and active region. The desired characteristic for improved efficiency is to have a low RC time constant during the charging period when the output voltage is lower than the input voltage. Conversely, a high time constant is desired during the charge leakage period. Therefore, to prevent the leakage currents, we want to decrease the resistance when the input is higher than the output so that the output

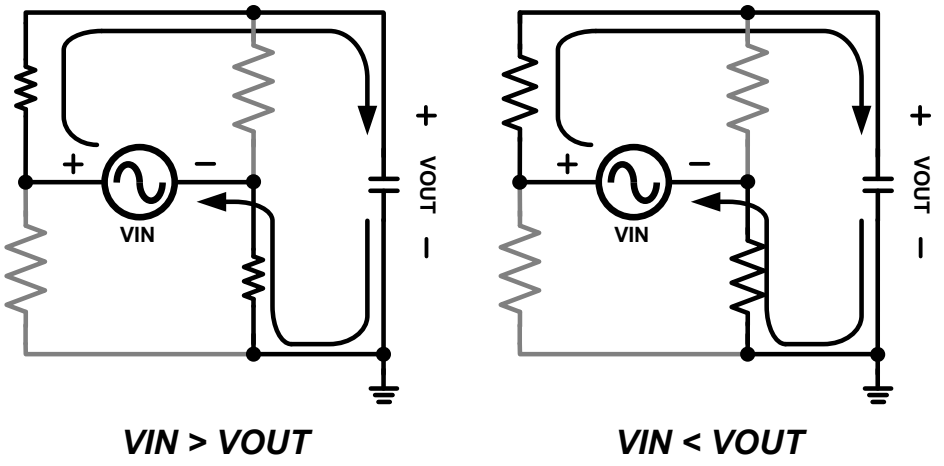


Figure 41: Leakage reduction strategy.

capacitor can be charged fairly well, while we want to maximize the resistance when the output is higher so that the leakage current is minimized as shown in Figure 41.

To adjust the time constant adaptively, the leakage control comparator is utilized as shown in Figure 42. This comparator takes one of the RF signals ($RF+$ or $RF-$) as its positive input and the rectified node as its negative input. Since the negative input also acts as a virtual supply, this comparator does not require an external supply. When $RF+$ (or $RF-$) is higher than $DC+$, the output of $CP1$ (or $CP2$) goes low. This reduces the RC time constant associated with $MRP1$ (or $MRP2$) and helps the charging process. Conversely, the RC time constant becomes higher when $RF+$ (or $RF-$) becomes smaller than $DC+$. In this case, $CP1$ (or $CP2$) raises its output voltage to decrease the gate drive voltage of $MRP1$ (or $MRP2$).

- **Active Body Biasing**

When we look at PMOS device, there are parasitic diodes connected to the body terminal. Thus, we want to make sure the body terminal is connected to the highest potential. However, as mentioned earlier, there is no stable supply voltage to tie up the body terminals of PMOS transistors. For example, when the body of $MRP1$ and $MRP2$ is tied to $DC+$, $RF+/RF-$ can be significantly higher than DC+ at the

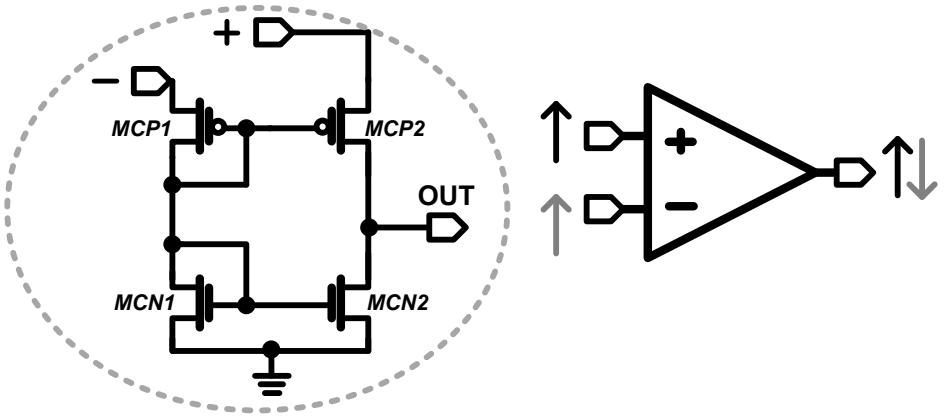


Figure 42: Leakage control comparator.

beginning of the rectifying operation. If this voltage difference beats the threshold voltage of the parasitic body junction diode, currents can flow into the body and damage the device as shown in Figure 43.

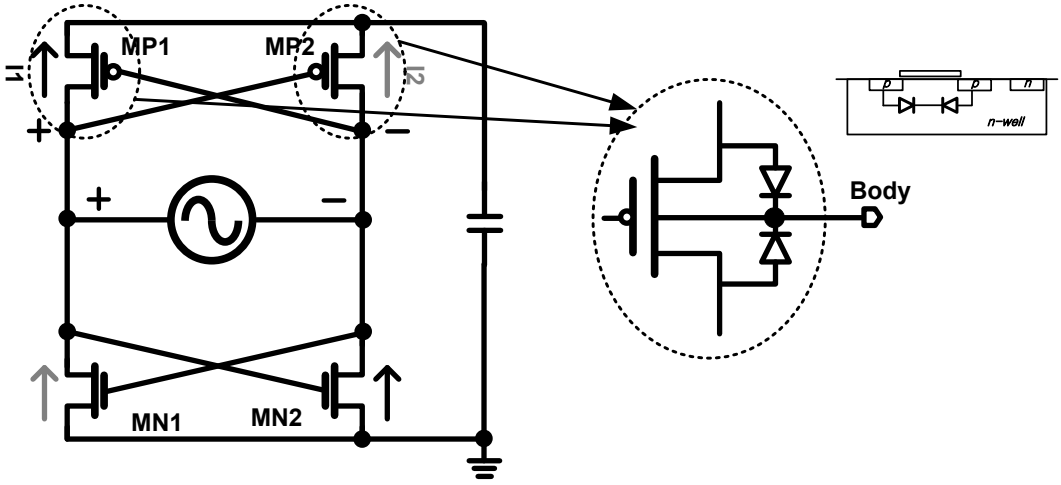


Figure 43: PMOS body connection issue.

Therefore, the adaptive body biasing cell shown in Figure 44 is applied to ensure the body of $MRP1$ and $MRP2$ is always tied to the higher potential of $RF+/RF-$ or $DC+$. The PMOS cross-coupled pair ($MBP1$ and $MBP2$) is connected to the body terminal in such way that the body terminal is connected to whichever the higher potential than the other.

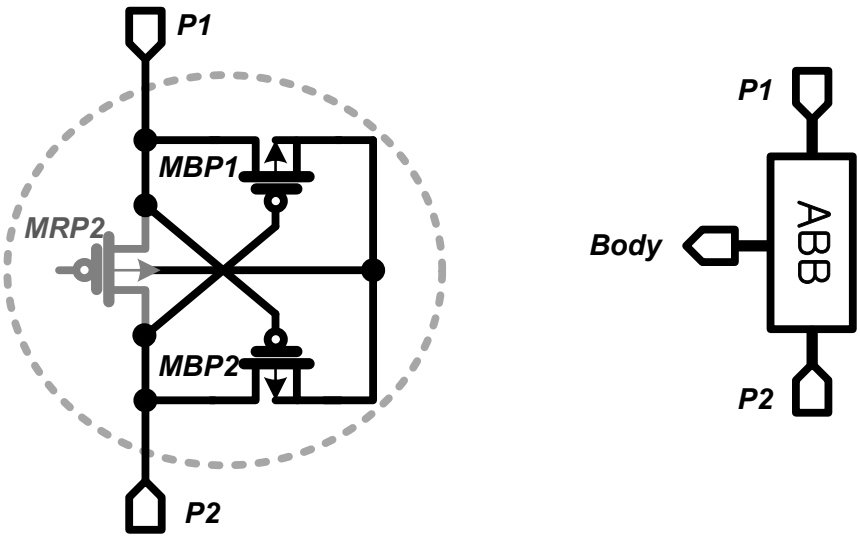


Figure 44: Adaptive body biasing cell.

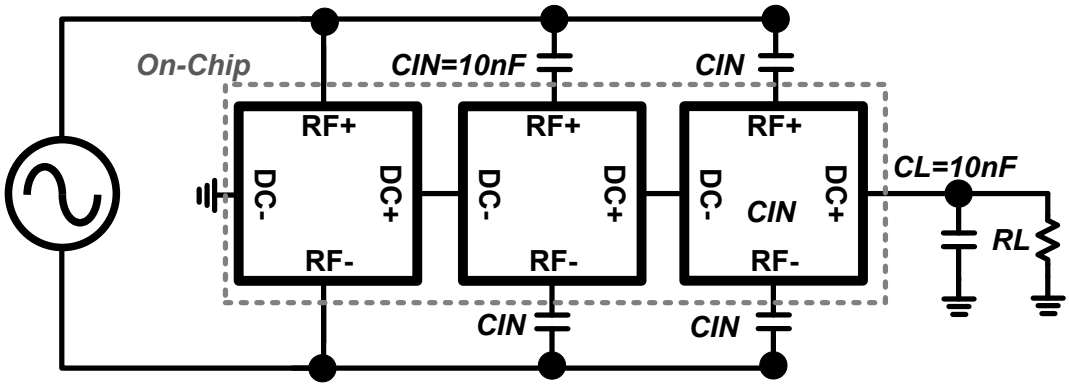


Figure 45: Measurement setup.

5.4.4 Experimental Results

Since the rectifier conversion ability is highly dependent on the size of transistors, which varies a lot depending on applications. Thus, the conventional rectifier and the proposed rectifier are implemented with the same transistor size for a fair comparison in 0.18 μm CMOS technology. The two rectifiers are in -three-stage configuration as shown in Figure 45, and the exactly same PCB and external component settings are applied to the two rectifier system. The die photos of the proposed and the conventional rectifier are shown in Figure 46.

Figure 47 shows a transient waveform of the inputs and outputs of the proposed

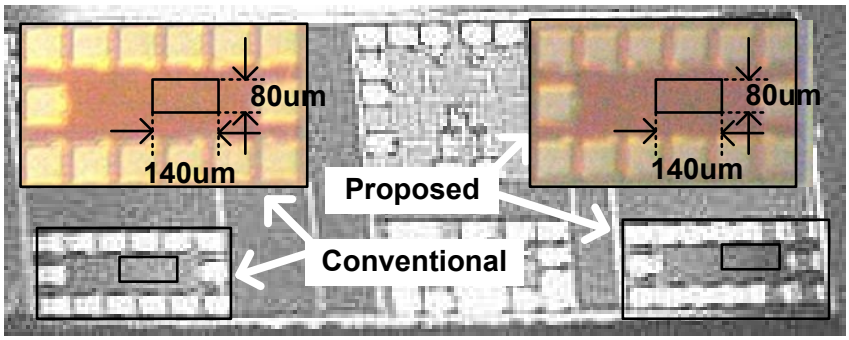


Figure 46: Die photo of the proposed and the conventional rectifier testchips.

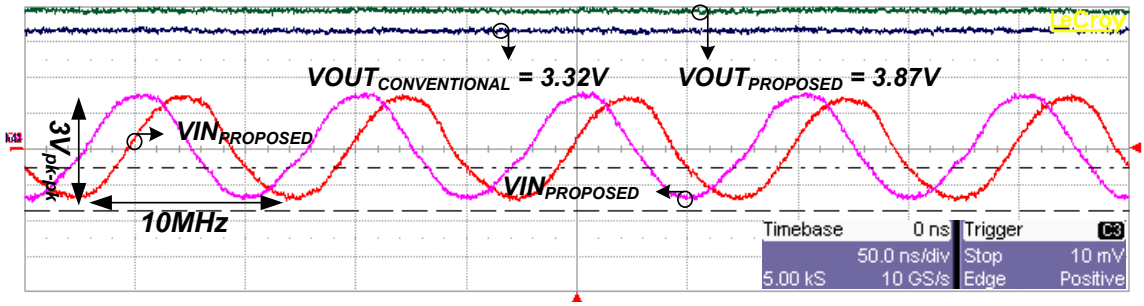


Figure 47: Measured voltage waveform of the proposed and the conventional rectifiers when VRFAMP = 1.5 V and f = 10 MHz is applied.

and the other rectifier when the input frequency and amplitude are 10 MHz and 3 Vpk-pk, respectively. As the proposed semi-active high-efficient CMOS rectifier prevents leakage currents, the amount of the leakage currents flowing in the conventional rectifier can be saved, and this leads to improved conversion efficiency. The output voltages were measured as the input amplitudes were swept as in Figure 48. The proposed rectifier shows approximately 15% higher voltage conversion efficiency.

5.4.5 Conclusion

For the power unit, the charge leakage issue in a CMOS full wave rectifier has been analyze, and a semi-active high efficient CMOS rectifier has been proposed and implemented to improve the conversion efficiency and reliability by preventing the PMOS body-junction diodes from turning on.

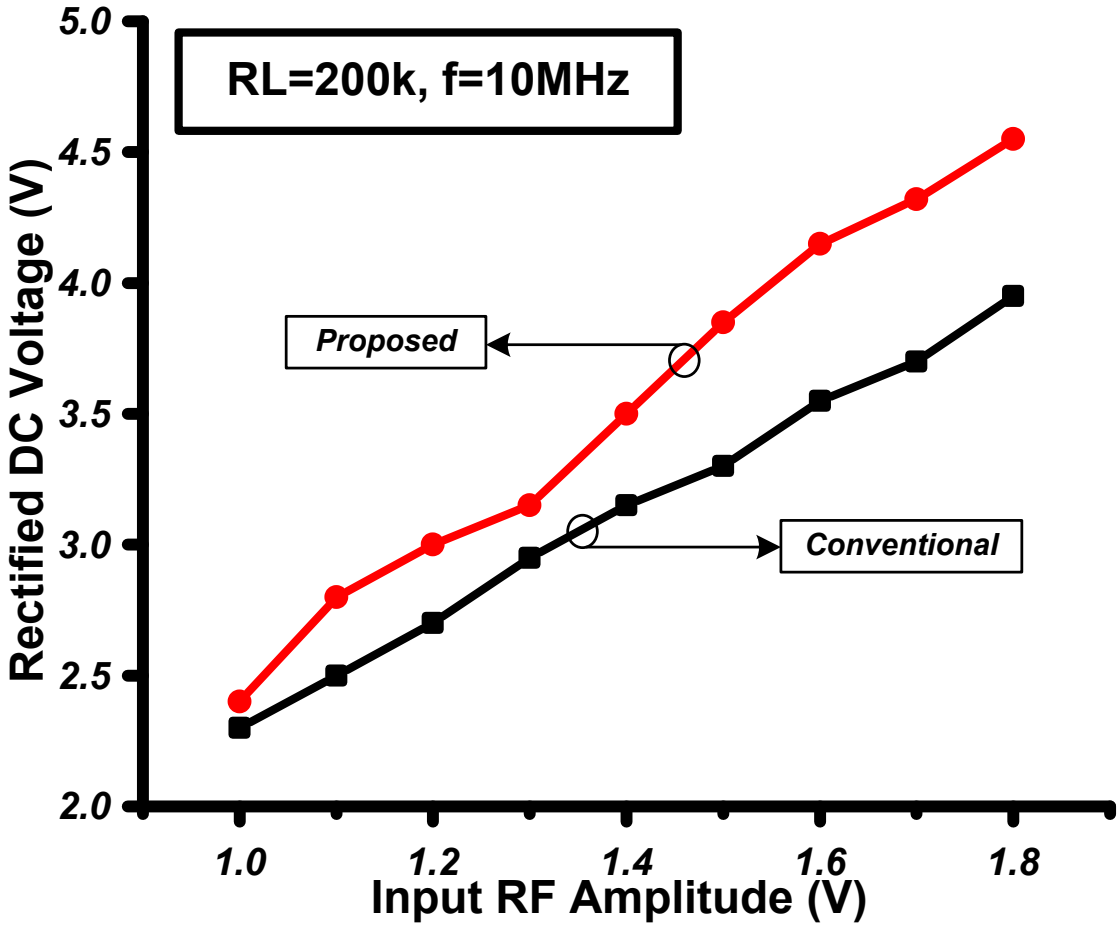


Figure 48: Measured DC voltages varying input amplitudes.

CHAPTER VI

LINK-VARIATION MONITORING FOR ENHANCED OPERATING EFFICIENCY

6.1 System Performance under Real Environments

Once a wireless sensor device is deployed, it must undergo variations in the operating condition. For example, changes in either the physical distance or orientation would attenuate or intensify incoming and output-going signals. Consequently, unless these inevitable variations are compensated, a wireless sensor device would consume unnecessary energy for a given task or too little energy to meet the requirement. Therefore, the operating efficiency will be different from the originally targeted value, and a link-variation sensing is an important procedure for the successful operation of realistic wireless sensor applications.

In the previous sections, circuit design methodologies that can improve the upper limits of the system efficiency in the signal processing, the memory, and the power units have been discussed. Although it is highly desirable to maximize the theoretical upper bounds, the maximum achievable upper bounds only cannot promise consistent performance under unpredictable changes in operating conditions.

In this chapter, a technique to evaluate link-variations which is due to the realistic deployments of a wireless sensor device is proposed to to analyze and develop a link-variation sensing technique that can evaluate operational disturbances such as component mismatches and displacement variations so that the performance of a wireless sensor device in the actual environment can be close to the optimum without wasting an excessive amount of energy. The proposed technique will be applied to an inductively-coupled wireless sensor to implement a variation-tolerable power

receiver. At the same time, the proposed technique will focus on generating digital values that are proportional to the amount of variations without interrupting the original function, and this digital evaluation can be used for the *in-situ* adaptive link compensation (ALC).

6.2 Inductively-Coupled Power Link and Link Compensation Concept

An inductively-coupled link can play multiple roles in wireless sensor applications. While it can be used as a part of an energy scavenging system, it can also function as a part of a sensor unit as well as a transceiver unit. When an inductively-coupled link forms the main energy channel between a wireless sensor device and its base station, the energy extractor unit severely undergoes the link-variations by which the performance of the energy extractor is directly affected. Therefore, the link-variation sensing technique can be validated in an inductively-coupled power transmission setup.

A number of wireless sensors including bio-implantable devices often utilize inductively-coupled wireless power transmission (WPT) due to its reliable and non-intrusive nature. Once the transmission frequency and distance is set, the upper limits of the inductively coupled power transmission efficiency depend on the quality of L-C resonant matching networks. Therefore, high-Q L-C matching is often used to increase the theoretical upper bound. However, once a device with WPT function is fabricated and deployed in real operating conditions, the matching network in the device suffers from link variations such as component mismatches between the primary and the secondary L-C networks and any physical environmental disturbances that might cause variations in mutual inductance between the two coils. Therefore, the actual WPT efficiency may not coincide with the theoretical limit. In fact, the operating efficiency will be determined by how close the present matching condition is to the optimum point as shown in Figure 49.

In [48], [24], and [34], adaptive link-compensating schemes have been proposed.

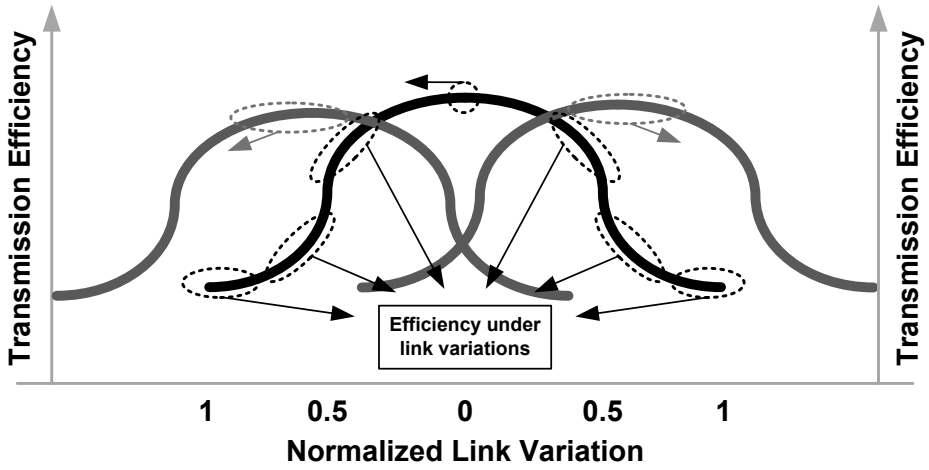


Figure 49: Operating principal of the adaptive link compensation (ALC).

However, in [48] and [24], results feature a fixed resolution determined by the physical size of the capacitor bank, and data/power transmission must be interrupted during compensation, and [34] requires external assessment block for link-evaluation. In this chapter, an adaptively tunable wireless power receiver with a non-interruptive link-variation-to-digital converter (LDC) is demonstrated.

6.2.1 Link-Variation Sensing and Evaluating Strategies

For the operation of the ALC, in which the resonant matching network is adaptively tuned can be divided into two steps, link variations have to be sensed and evaluated. During the link variation sensing, the main signal flow should not be interrupted, and any energy invested in the link evaluation must be significantly lower than the improvement in the overall energy gain after the link tuning. If these two features are valid, we can say that efficiency under the realistic link-variations is improved with the use of ALC.

For the variation sensing, there can be two methods as shown in Figure 50. The water flow rate implies the energy flow rate, the intensity of which is proportional to how close the current operating condition is to the optimum point. The water bucket corresponds to a capacitor that stores the wireless energy. In Method I, the time for

Figure 50: Conceptual analogies of link variation sensing methods.

the current water faucet setting, or the current matching condition to fill the bucket is measured, and the bucket is emptied for the next variation sensing. It leads a straightforward implementation but during the variation sensing, the signal flow has to be dedicated for the sensing. In the meanwhile, Method II samples a small portion of the incoming energy flow so that the majority of the signal flow can still be used towards the original purposed. However, it requires a special sampling circuit block.

During the link evaluation, if the amount of the invested energy can be adjusted depending on the achievable energy gain after the link-tuning, the energy gain can be further enhanced. For an application having a high time constant of link-variations, the energy investment should be regulated so that the overall energy gain is still positive. On the other hand, for relatively slow changing link-variations, more energy can be consumed for more precise link-evaluation which would result in higher energy gain as shown in Figure 51.

The proposed LDC does not interrupt energy harvesting during the link evaluation by adopting a novel signal sampler and can adjust the amount of energy investment in the link-evaluation by using a multi-resolution digitizer.

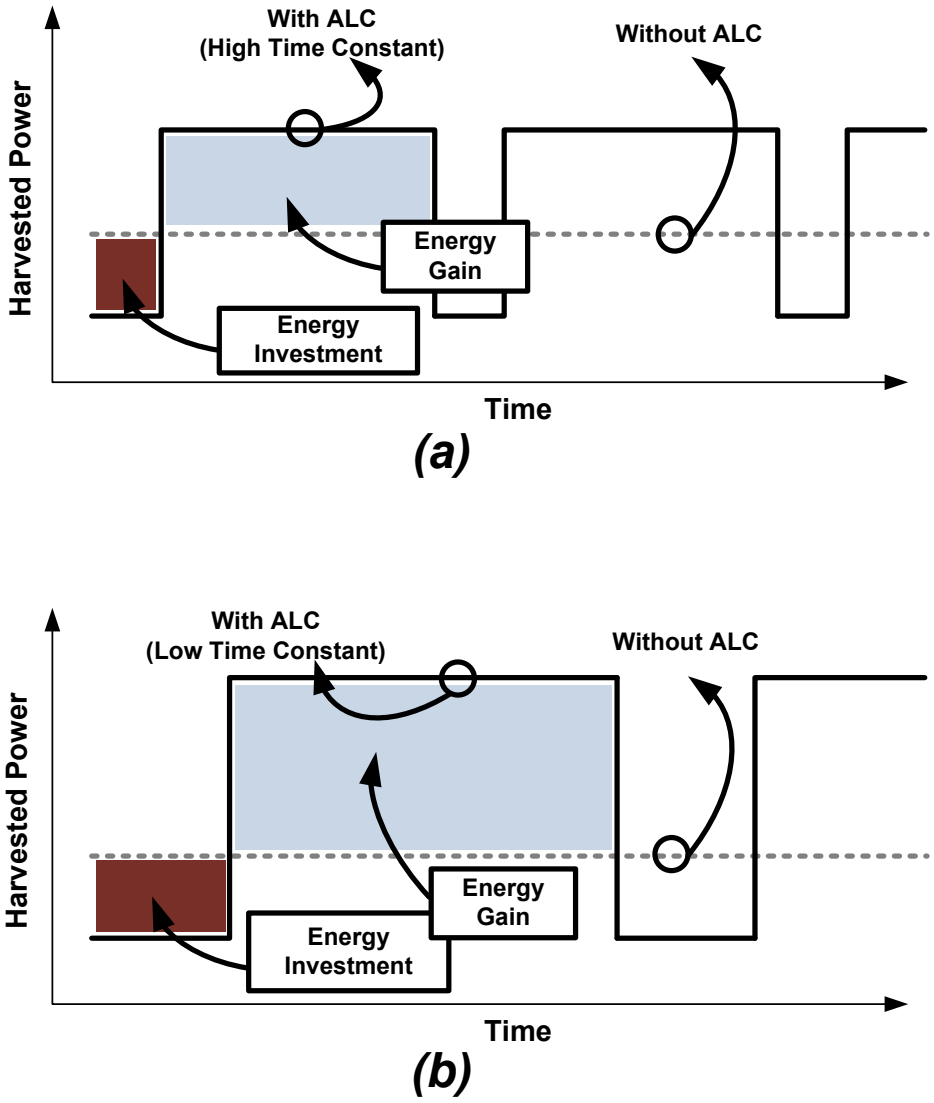


Figure 51: Conceptual time domain diagram of harvested power with and without the adaptive link compensation for (a) high time constant and (b) low time constant.

6.3 Proposed Link-Variation-to-Digital-Converter

Figure 52 shows the block diagram of the proposed LDC attached to a conventional wireless sensor device, which often includes a modulator and a demodulator for communication, a processing unit, a sensor unit, and a power management unit shown in gray solid lines. The link evaluation should have minimal disturbance on the original system functionality, and the outputs are preferred in digital. To achieve these goals, a non-inverting buck-boost power chain and a multi-resolution counting analog-to-digital converter (ADC) have been adopted in the proposed LDC.

6.3.1 Signal Sampler

The buck-boost chain consists of switches ($M1$, $M2$, $M3$, and $M4$), an inductor (L), and a hysteresis comparator. When C_{IN} is charged beyond the hysteresis comparator turn-on threshold voltage, Phase I begins as shown in Fig. 2. During Phase I, the comparator closes $M1$ and $M3$, and some of the charges in C_{IN} are discharged through L. As L gets energized, C_{IN} loses its charges, and V_{IN} decreases. When V_{IN} is below the turn-off threshold voltage, the comparator opens up $M1$ and $M3$ and closes $M2$ and $M4$ (the beginning of Phase II). During Phase II, the previously energized L dumps its remaining magnetic charge to C_{AUX}. When V_{IN} charges up beyond the switching threshold, Phase II ends, and Phase I repeats.

As link variations influence the charge flow rate in C_{IN}, the buck-boost chain translates the charge flow rate into a ratio of a Phase I duration, ton, to a Phase II duration, toff; since the charge injection originates from the voltage multiplier, the sum of the two duration stays constant. From the principle of inductor volt-second balance [12], we can see that V_{AUX} is strongly correlated with link-variations.

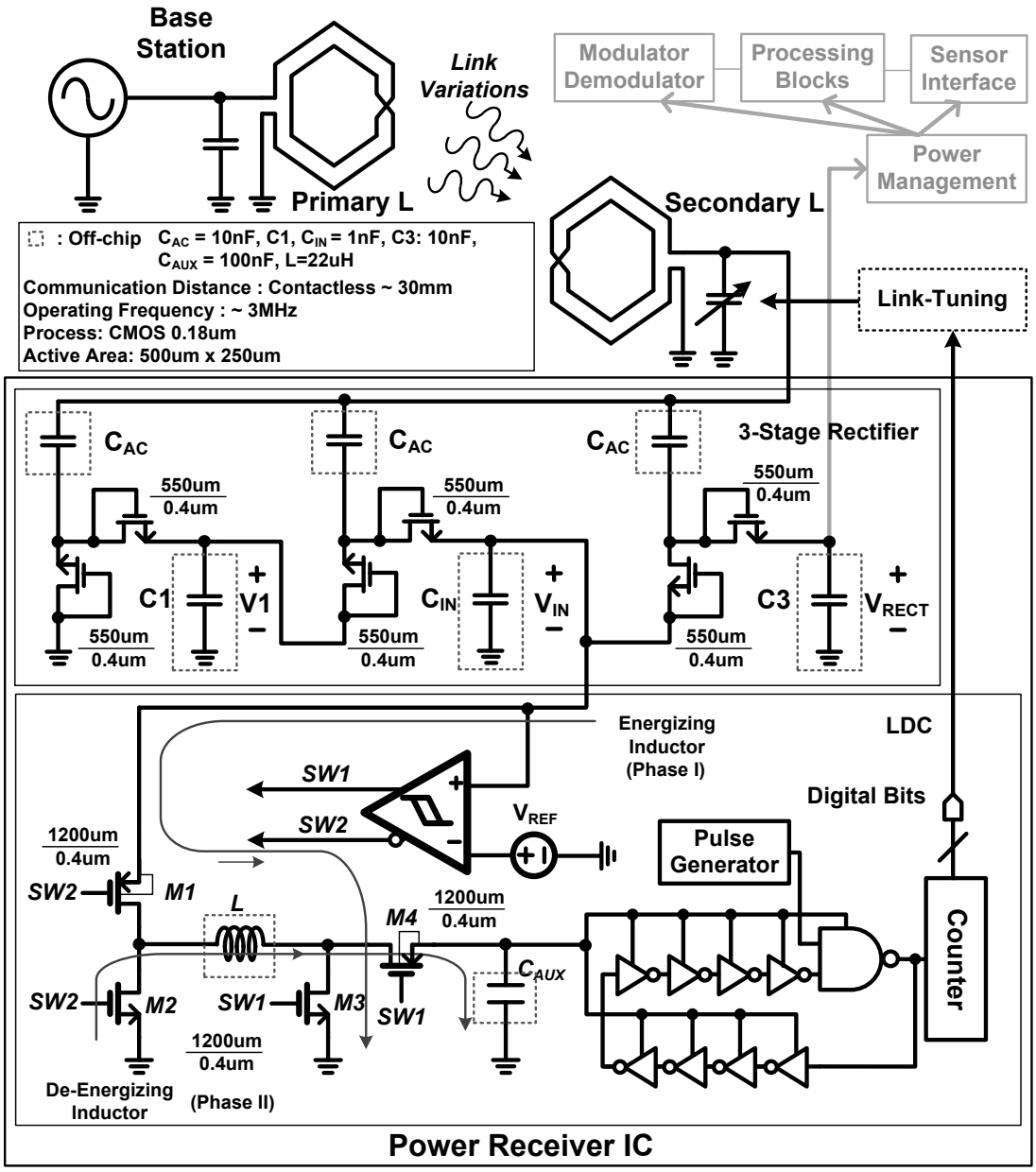


Figure 52: Block diagram of a tunable power receiver prototype with the proposed LDC in an inductively coupled wireless sensor system.

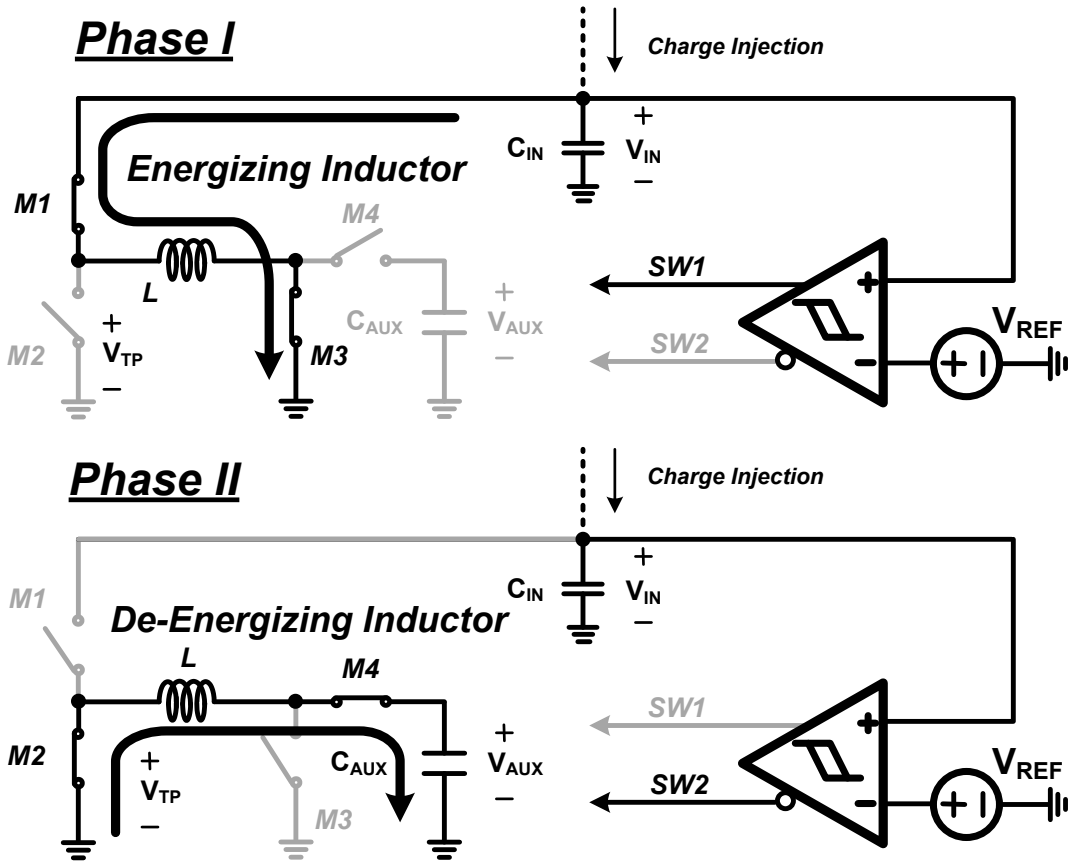


Figure 53: Operating mechanism of the LDC power chain.

$$\frac{V_{IN}t_{on}}{L} = \frac{V_{AUX}t_{off}}{L} \tag{22}$$

$$V_{AUX} = \frac{t_{on}}{t_{off}}V_{IN} = \frac{D}{1-D}V_{IN} \tag{23}$$

$$D = \frac{t_{on}}{t_{on}+t_{off}} \tag{24}$$

, where V_{IN} is proportional to the charge flow rate.

6.3.2 Digitizer

The digitizer in the LDC is realized with a ring oscillator and a digital counter. The supply of the oscillator, which consists of eight inverters and a NAND for an enable function, is connected to V_{AUX}. The oscillation frequency is proportional to V_{AUX}, and the counter converts the frequency into a digital code that represents the strength of V_{AUX}. The counting duration is controlled by the width of a pulse from the pulse generator. This duration determines how much energy should be invested for the link-evaluation; a longer period of counting can result in a finer resolution.

6.4 Power Receiver Prototype

The tunable power receiver prototype consists of an off-chip tunable L-C network, a three-stage rectifier, and a proposed LDC block. The L-C network is realized with a flexible printed circuit board (FPCB) inductor and film-trim capacitors. The FPCB inductor was designed to have Q-factor above 100 and inductance of 15 μH. The physical dimension of the FPCB inductor is about 45 mm-by-45 mm. For the prototype verification, the same FPCB inductors are used for the primary and the secondary coils. The three-stage rectifier is implemented with diode-connected transistors and forms the main energy path.

The amount of DC energy harvested at C3 will be affected by the link-variations in the inductively coupled link; mismatches in the resonant matching networks and

inductor misalignments would be major cause for the link-variations. Therefore, with the power receiver prototype, realistic link-variations can be emulated and the functionality of the proposed LDC can be tested. Since the buck-boost power chain in the LDC isolates the remaining evaluation blocks from the main energy path, the input energy can be continuously harvested even during the link-evaluation. After the evaluation, the LDC is disabled, and the evaluation results are applied to the link-tuning operation in which a simple binary algorithm adjusts the off-chip tunable capacitor banks.

6.4.1 Transfer Function

Figure 54 shows simplified block level transfer functions for the proposed LDC. The proposed LDC first senses a link variation profile assuming resonant matching is a dominant factor for overall efficiency degradation. Then, AC-to-DC conversion occurs at the rectifier. At the signal power of interest, it is reasonable to assume the voltage conversion rate stays constant. As the voltage conversion rate is constant, the signal at the input of the buck-boost power chain follows the input link variation profile, which has a concave shape around the optimum tuning point. The following buck-boost power chain has a transfer function of $\frac{D}{1-D} \times V_{IN}$, convex shape, and the maximum input charge rate occurs at the optimum tuning point. Therefore, the output voltage, V_{AUX}, of the buck-boost power chain exhibits triangular shape. Finally, the digitizer can have higher gain by increasing the counting period, which results in finer resolution.

6.4.2 Process-Temperature Variation

The absolute output results of the LDC are prone to process and temperature variation. However, for link variation sensing, we are using the relative changes in the output codes for different matching/input conditions rather than the absolute values. As long as the transfer functions of the buck-boost power chain and the digitizer

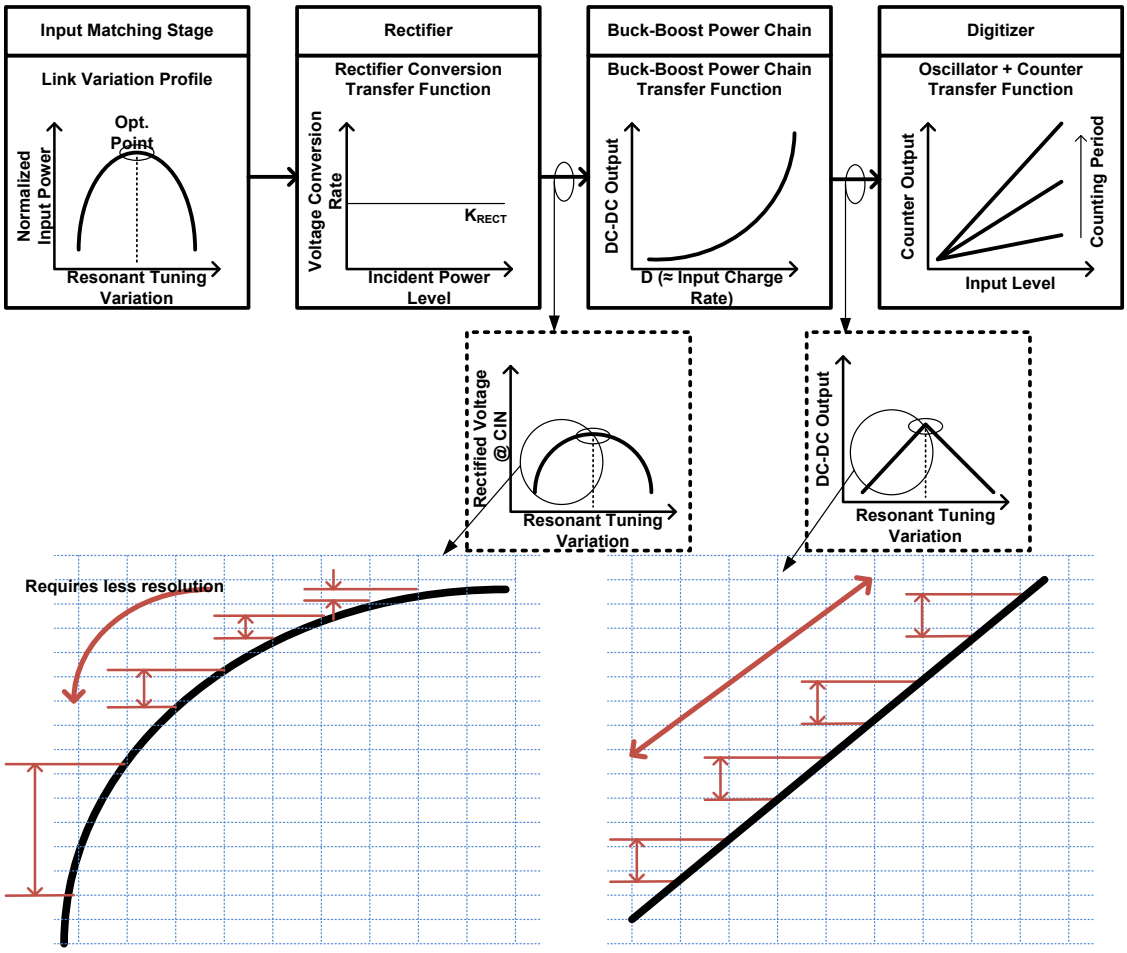


Figure 54: Simplified block level transfer functions for the proposed LDC.

maintain monotonic increasing behaviors, performance variations from one sensor to another can be tolerated. In other words, as long as LDC's generate the highest output code for the optimum input condition or the highest possible input power level and the lowest output code for the worst input condition, the relative output codes of LDC's are valid.

Process variations show stochastic distribution determined by the given fabrication process. The consequence of process variations is often mitigated by using larger area but still hard to control at design stage. On the other hand, we can estimate the effects of temperature variations on the output frequency of the ring oscillator. The output frequency of an inverter-based ring oscillator is a strong function of mobility and threshold voltages. As the junction temperature increases, mobility tends to degrade while threshold voltages tend to decrease. For a higher oscillation frequency, mobility needs to be high and threshold voltages need to be low. If a supply voltage is chosen to be much higher than threshold voltages, the impact of threshold voltage variations will be smaller than that of mobility variations. As a supply voltage decreases, the impact of threshold voltage variations gets stronger. Therefore, if we chose an adequate supply voltage range, the temperature variations on the oscillation frequency can be minimized.

In the proposed LDC, the ring oscillator consists of eight inverters and a NAND gate. The frequency variations over process and temperature for a supply voltage of 3.3 V, 1.2 V, and 1 V are shown in Figure 55. For a 3.3 V supply, the output frequency decreases with temperature due to the mobility degradation. For a 1.2 V supply, the impact of mobility variations and that of threshold voltage variations become comparable. Therefore, the output frequency is less sensitive to overall temperature variations. For a 1 V supply, the impact of threshold voltage variations becomes dominant and the output frequency increases with temperature.

Although we tried to locate the ring oscillator supply voltage less than 1.2 V, the

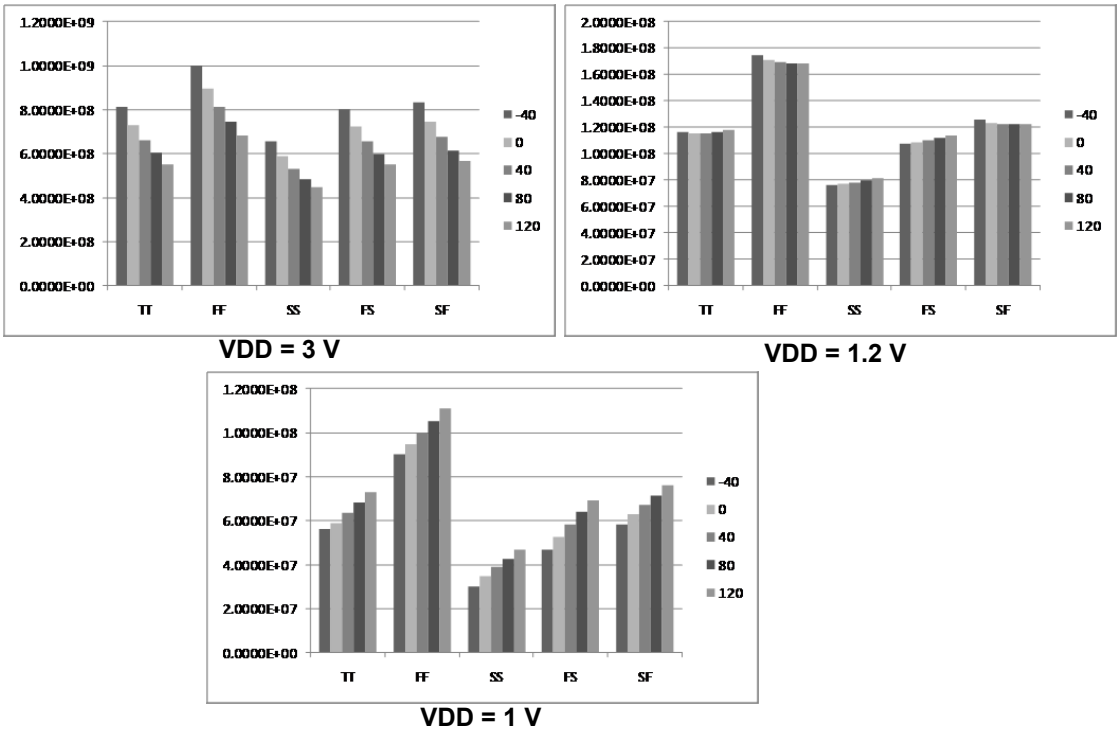


Figure 55: Ring oscillator frequency variations when 3.0 V, 1.2 V, and 1 V supplies are used.

variations in the oscillation frequency due to process and temperature are inevitable. However, as the tuning algorithm does not depend on the absolute value of the digital codes translated from the ring oscillator frequency, the PT variations will not have a major impact on the effectiveness of the capacitance tuning algorithm. The resolution of the LDC would be affected by the PT variations; if the output frequency decreases due to the PT variations, the resolution will be degraded. However, by having a flexible counting duration, the resolution of the proposed LDC can be adjusted.

6.4.3 Link-Tuning

Figure 56 shows an example of the capacitance tuning process. Assuming we have binary weighted capacitor bank. We can start from the minimum capacitance value. As we increase the capacitance bank register (Set_Temp), we can compare the current LDC output code (LDC_OUT) to the previous output ($Temp$). If we chose the larger

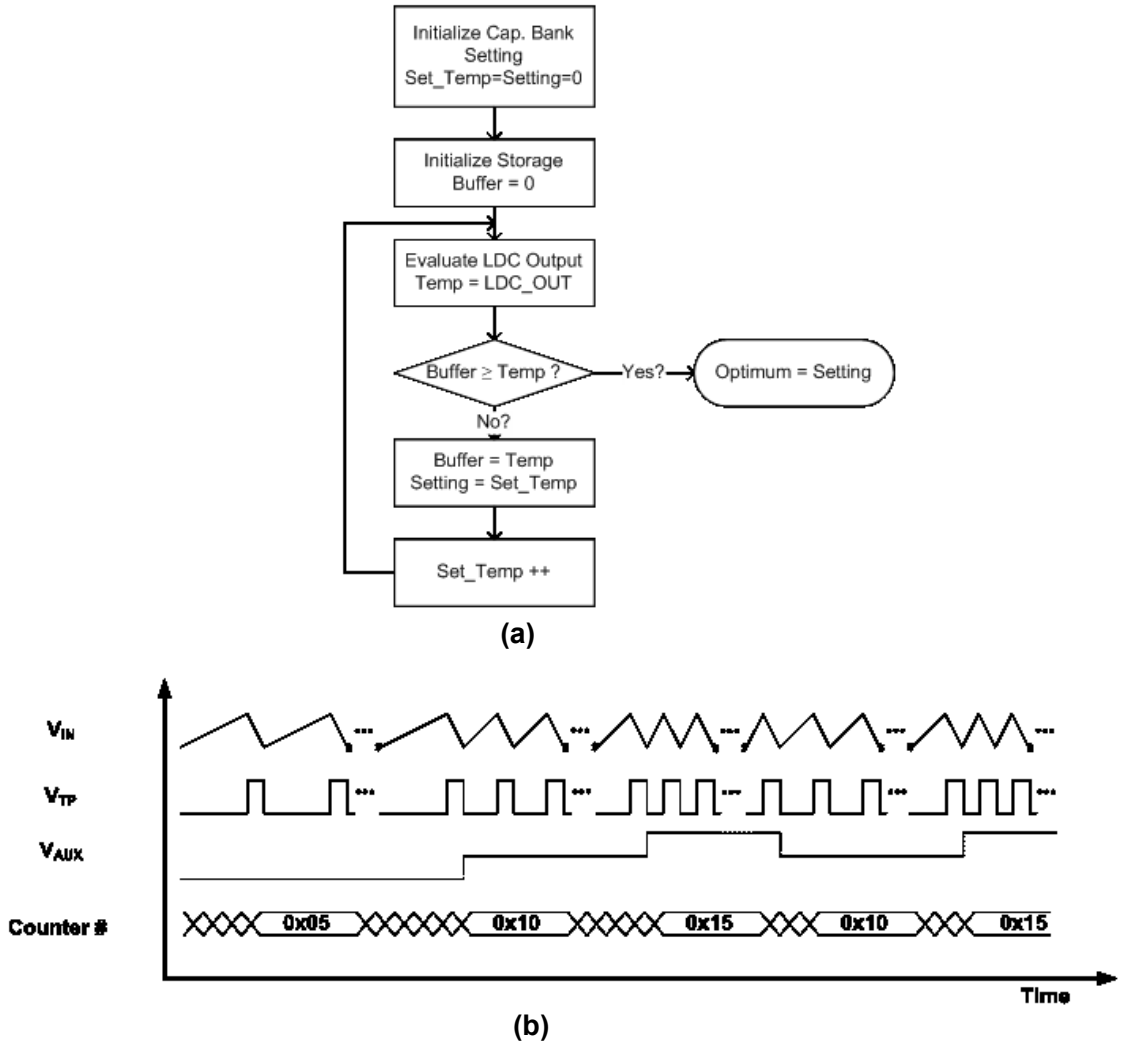


Figure 56: Conceptual diagram of the capacitance-tuning process in (a) a flowchart and (b) a time-domain waveform.

one between the two, we can find the best capacitance tuning value.

6.5 Measurement Results

The combination of the FPCB inductors and the capacitor banks has a resonant frequency range of 1 5 MHz. Figure 57 shows the power chain output, V_{AUX}, and the corresponding duty cycle waveforms, V_{TP}, for three input amplitudes, 2.4 Vpk-pk, 2.0 Vpk-pk, and 1.6 Vpk-pk, applied to the prototype.

To characterize the transfer function of the buck-boost power chain, which plays

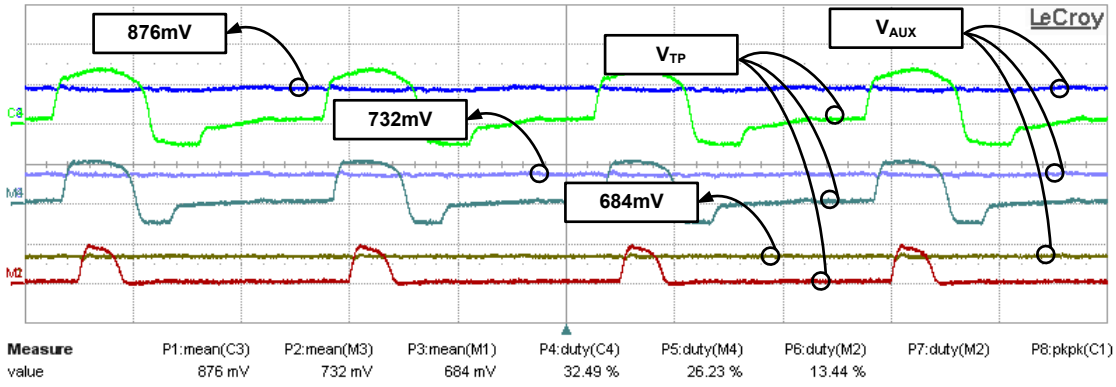


Figure 57: Duty cycles and power chain output voltages for 2 MHz input AC amplitudes of 2.4, 2.0, and 1.6 Vpk-pk applied to the power receiver.

the essential role of the link evaluation, the voltage amplitude at the power receiver prototype are varied while the output of the proposed LDC are observed. In this way, without involving any link variation profile, the input signal versus the output of the LDC can be characterized. In addition, by changing the pulse width at the output of the pulse generator, the multi-resolution functionality of the proposed LDC can be verified. Figure 58 has the three-stage rectifier output voltages versus LDC output curves, and the counting pulse widths of each curves are 2.5 μs, 5 μs, and 10 μs. Since the digitizer in the LDC consists of a ring oscillator and a digital counter, the higher counting period is, the finer input amplitude can be differentiated.

The output codes from the proposed LDC might not be distinguished under weak conditions. However, the LDC can adjust the link evaluation period for finer resolution, which corresponds to increasing the counting duration of the digitizer. As we increase the counting duration from 2.5 μs and 10 μs, the minimum distinguishable rectifier output voltages under the weak condition improves from 250 mV to 17 mV shown in Figure 59.

As we are utilizing near-field inductive-coupling transmission with the identical transmitter/receiver coil diameter of 45 mm, the achievable communication distance was ranging from contactless to 30 mm. As the main focus of this power receiver

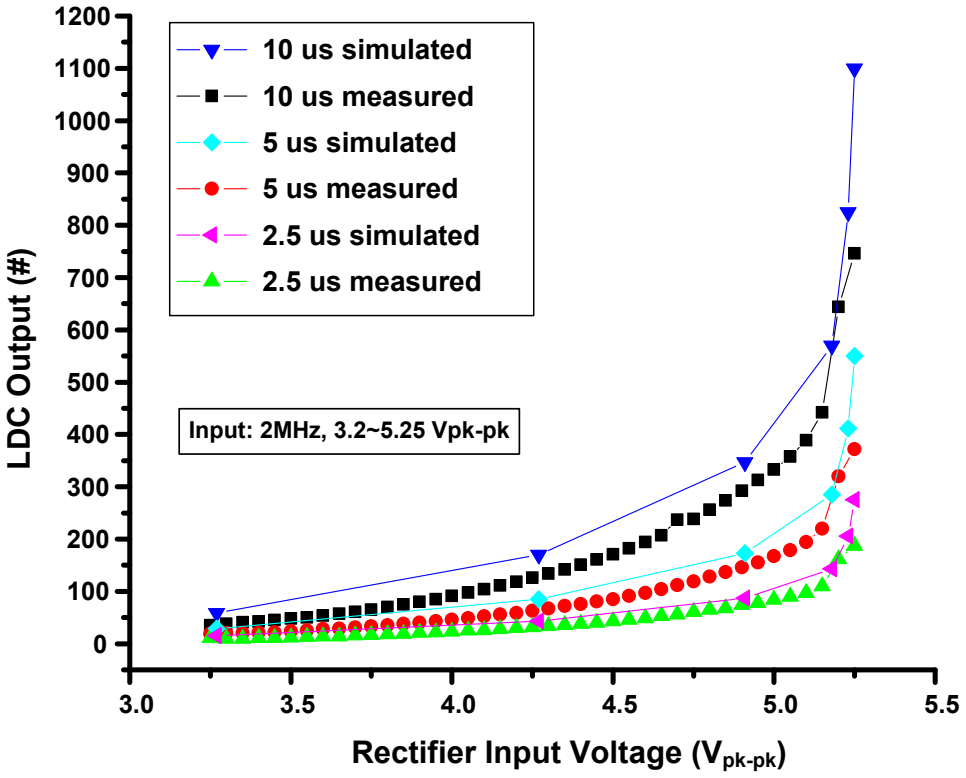


Figure 58: LDC outputs when 2 MHz sinusoidal signals with 3.2 5.25 Vpk-pk are applied to the input of the rectifier.

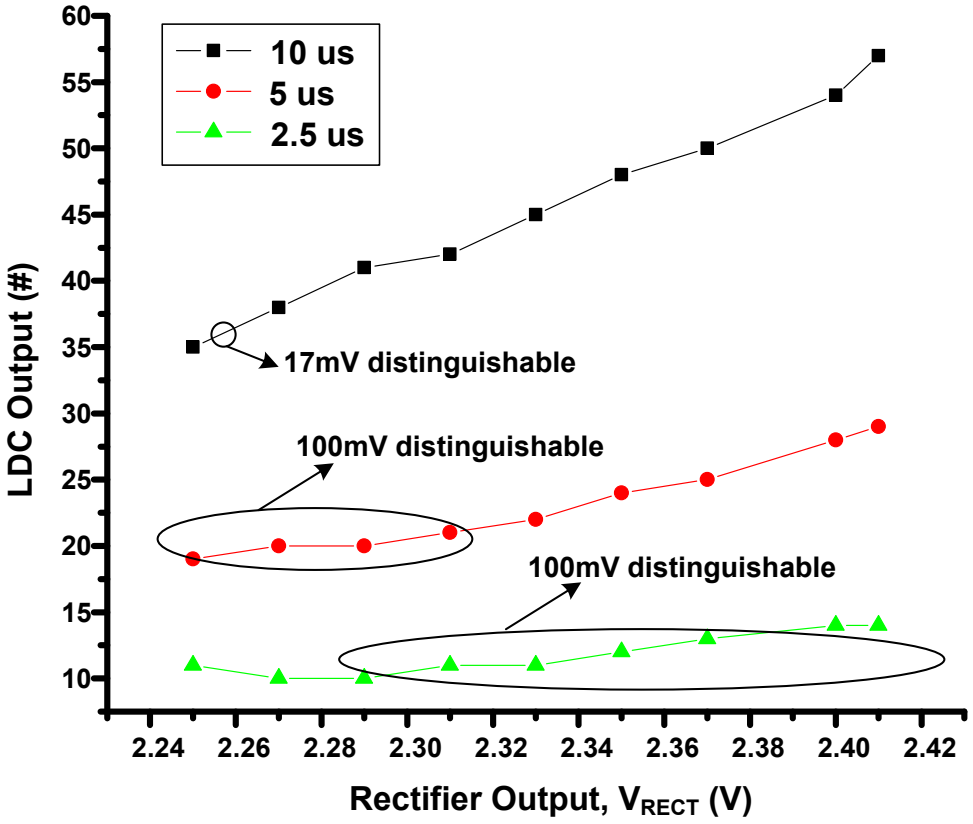


Figure 59: Rectifier output versus LDC output when 2MHz input signals with 3.2 3.65 Vpk-pk are applied the input of the rectifier.

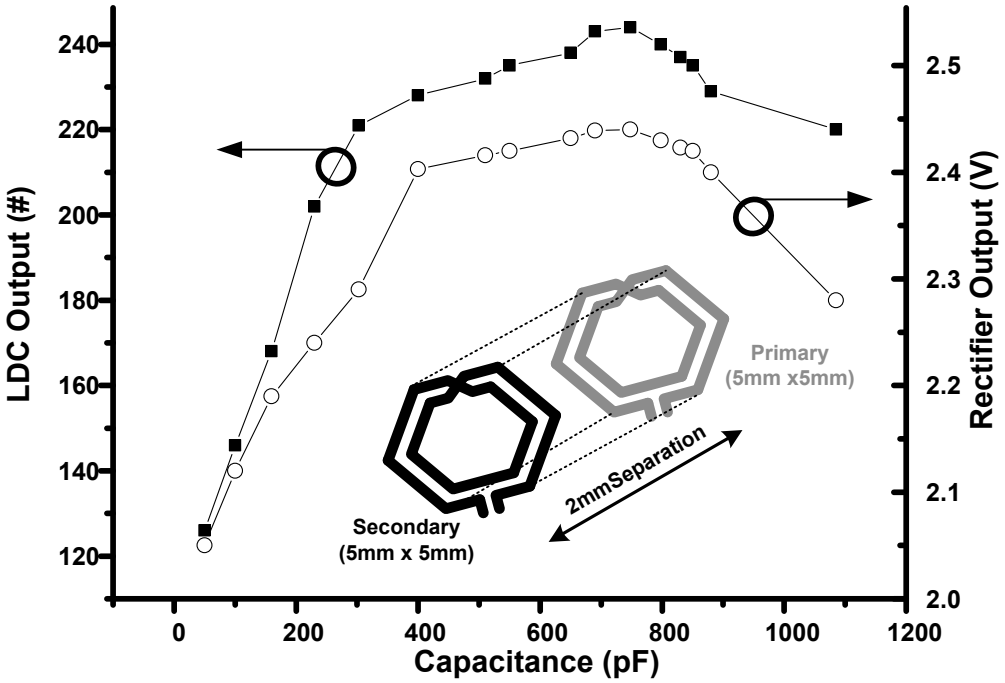


Figure 60: Tuning capacitance value versus LDC digital outputs and corresponding rectifier output voltages.

prototype is to verify the validity of the proposed LDC rather than the power transmission capability of the power receiver prototype, the 2 mm distance was chosen to configure well-controlled test conditions. Even slight angular disturbance in the transmitter/receiver coil pair would result in different transmission efficiency. Although the angular disturbance can be sensed by the proposed LDC, we eliminated any possible angular disturbance by attaching the FPCB inductors on transparent plastic flat plates with 2 mm thickness. To verify the link-evaluation capability under component mismatches, a 2 MHz signal is transmitted through a fixed primary resonant network to a 2 mm-away secondary resonant network, and the rectifier voltages and the LDC outputs are measured with various tuning capacitor values in Figure 60.

Realistic operating environments would involve mismatches in not only the resonant frequency matching but also the physical alignment of the primary and the secondary coils. For applications where the physical appearance of the secondary coil

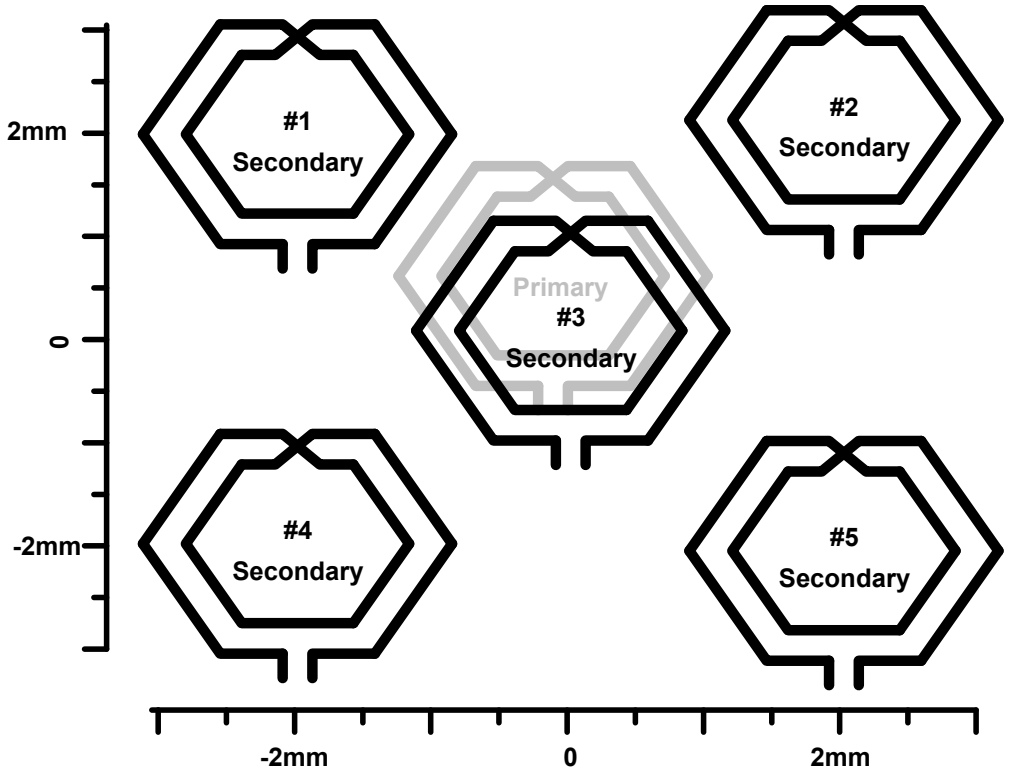


Figure 61: Inductor misalignment setup.

is not visible, the probability for the primary-to-secondary coil misalignment will increase. Changing the inductor alignment would result in different mutual inductance value, and the optimum tuning capacitance value has to be re-adjusted. We did not put our serious efforts on estimating the variations in the mutual inductance between the primary and the secondary FPCB inductors as it is beyond the main scope of this research topic. However, to emulate realistic inductor misalignment situations, the proposed power receiver was tested with five different inductor alignments as shown in Figure 61, including the near perfect alignment as indicated by #3, and four other misalignments as indicated by #1, #2, #4, and #5 as shown Figure 62. While the coordinate of the primary inductor is fixed, the secondary inductor is offset by 2 mm distance in either/both X-direction and Y-direction. For the inductor misalignments, the LDC outputs are measured with various capacitor values, as shown in Figure 63.

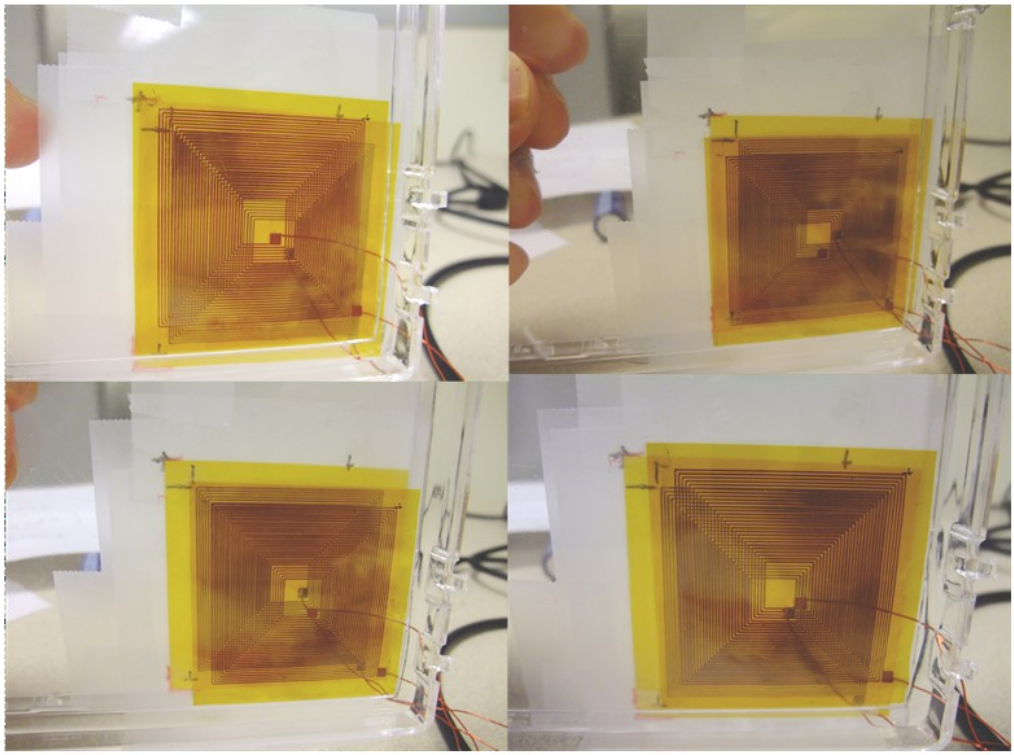


Figure 62: Photo examples of the inductor misalignment setup.

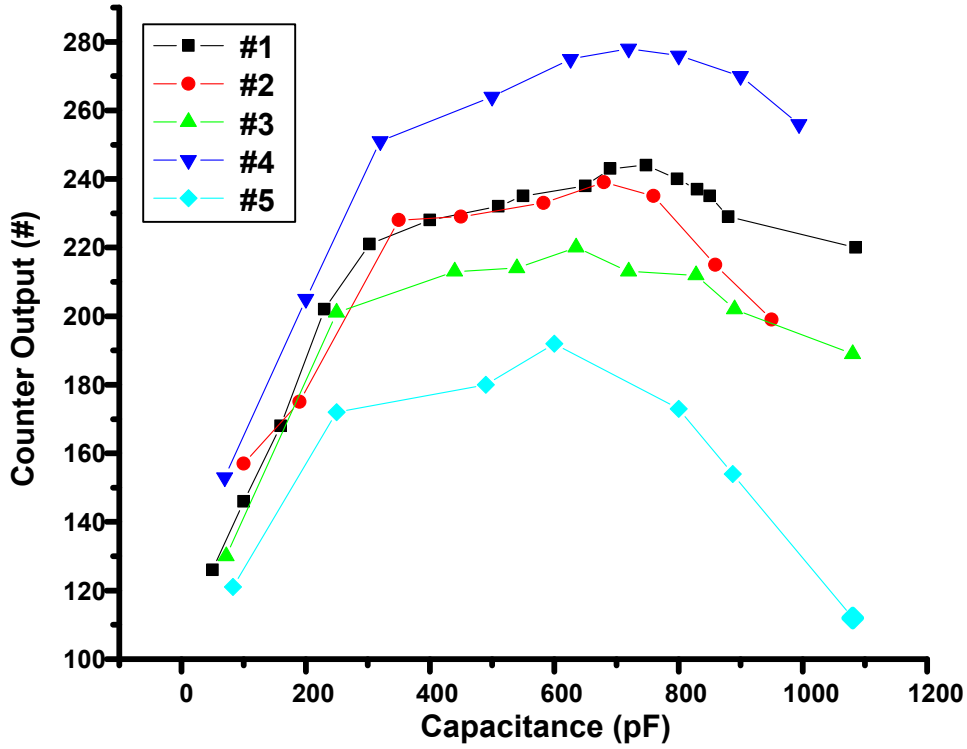


Figure 63: Tuning capacitance value versus LDC digital outputs under various inductor misalignments.

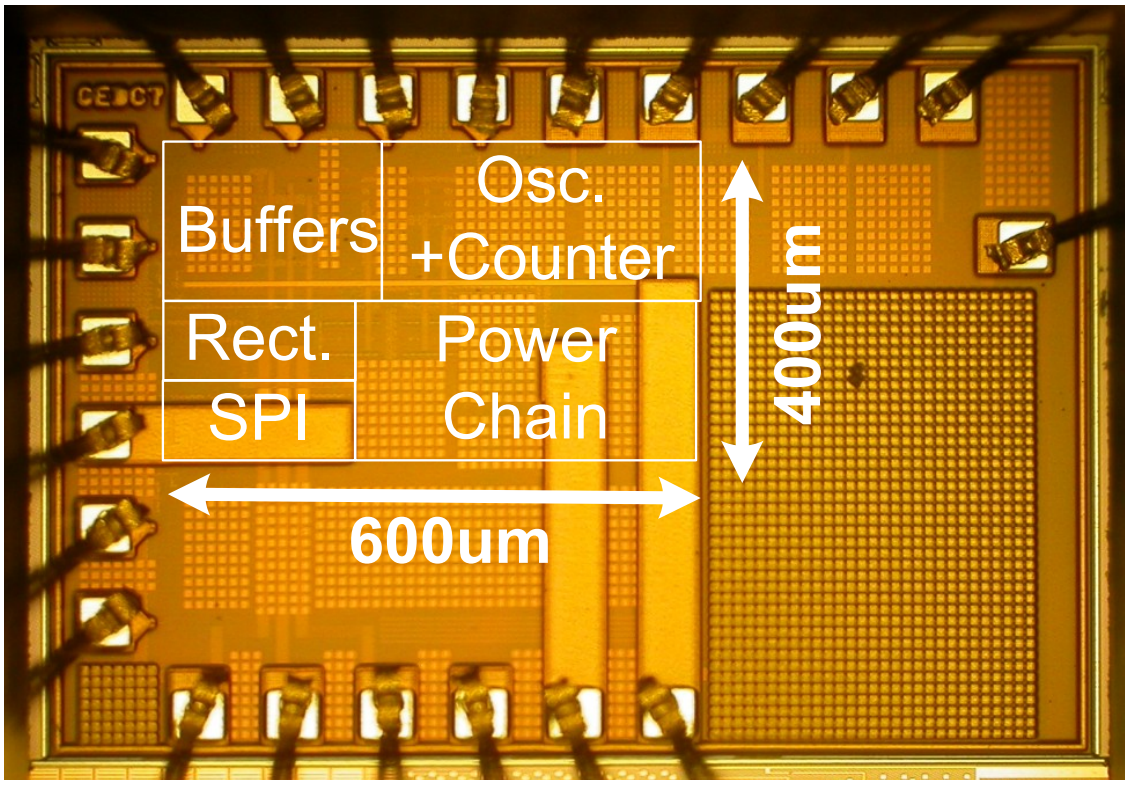


Figure 64: Die micrograph of the power receiver prototype.

The active area of the prototype, implemented in CMOS 0.18 μm, is 500 μm-by-250 μm. Figure 64 shows the die photo of the prototype.

6.6 Conclusion

In practical wireless sensor applications, unpredictable variations in the wireless link inevitably degrade the overall system performance. Evaluating the link variations in real-time is highly desirable for more reliable and efficient operations. This work presents a unique non-interruptive link-variation sensing technique that can provide *in situ* multi-resolution assessments.

CHAPTER VII

CONCLUSION AND FUTURE WORKS

7.1 Technical Contribution and Impact of the Dissertation

The objective of the proposed research is to analyze and develop energy optimized design techniques as well as a link-variation sensing technique that can improve the operating efficiency for a wireless sensor device.

Depending on applications needs, wireless sensor devices have to observe and sometimes interact with ambient physical phenomena such as pressure, brightness, and temperature while not disturbing their surroundings both physically and operationally. Conforming to the non-obtrusive requirement implies being operational for an extended period of with limited energy and hardware resources. In order to improve the operating efficiency under this harsh design constraint, energy-optimized design techniques are required for the essential functional blocks in a wireless sensor devices: the signal processing unit, the memory unit, and the power unit. Each block has its own requirements and design challenges.

In addition, after wireless sensors are deployed, the operating conditions will undergo unpredictable changes. Unless variations in the operating conditions should be properly observed and compensated, the deployed devices would consume either too little or too much energy to perform the given tasks.

Therefore, throughout the research, design strategies and some new circuit topologies are discussed to improve the operating efficiencies for the essential functional blocks in a wireless sensor device, and a novel link-variation sensing technique is proposed to make a wireless sensor for more reliable and efficient operations under unpredictable operating conditions. The contributions of this research are as follows:

1. A subthreshold analog computation system as an example of an energy-efficient analog signal processing system is designed and implemented. This system shows possibility that the analog signal processing can replace the complex and power-hungry digital signal processing in energy-constraint applications.

2. The leakage issues in SRAM is analyzed, and a new fully-gated 10T SRAM cell is proposed to reduce data-dependent leakage currents. When high memory capacity and low leakage power consumption features are critical design specifications, the proposed cell can be one of the best candidates.

3. The charge leakage problem in CMOS rectifiers is analyzed and a semi-active rectifier is proposed and implemented to improve the conversion efficiency by reducing the reverse charge leakage and reliability by preventing the PMOS body-junction diodes from turning on.

4. In practical wireless sensor operations, variations in operating conditions degrade the actual operating efficiencies. A novel LDC is proposed and implemented to enhance the operating efficiency. The proposed LDC, implemented along with a conventional three-stage rectifier in CMOS 0.18 μm, provides a unique non-interruptive multi-resolution link-variation sensing capability.

7.2 Scope of the Future Research

In this dissertation, circuit design techniques in the signal processing unit, the memory unit, and the power unit in a wireless sensor device are investigated for enhanced energy efficiency. In addition, a link-variation sensing technique that can contribute improving the operating efficiency under unpredictable variations is proposed.

For the signal processing unit, although the analog signal processing concept can bring significant improvement in terms of energy consumption, there remain major challenges in implementing low power, yet high accuracy mixed signal circuits, mainly

analog-to-digital converters and digital-to-analog-converters in ultra deep submicron technology. Also, efforts in improving digital domain blocks have to be continued. Subthreshold digital circuit design has been a popular method in energy-constraint applications, and a number of research activities focus on designing subtreshold digital circuits. However, generating subtreshold power supply voltages with high efficiency would still need some active research efforts and be one of the future research topics.

For the memory unit, this research focused on the memory cell. However, as wireless sensor applications have unique design requirements, there is a room for improvement in the memory controller and the sense amplifier.

For the power unit, this research focused on analyzing and improving a CMOS rectifier. To conserve already-restricted energy, energy-efficient power distributing methods have to be included in the future research. In addition, a power unit that can utilize multiple energy extractors should be considered.

In the area of the adaptive link compensation, integrating tunable passive blocks for the link tuning and implementing energy efficient tuning system are additional design challenges, and will be the extension of this research.

REFERENCES

[1] Akin, T., Najafi, K., and Bradley, R., "A wireless implantable multichannel digital neural recording system for a micromachined sieve electrode," *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 1, pp. 109–118, 1998.

[2] Akyildiz, I., Su, W., Sankarasubramaniam, Y., and Cayirci, E., "Wireless sensor networks: a survey," *Computer networks*, vol. 38, no. 4, pp. 393–422, 2002.

[3] Alvandpour, A., Somasekhar, D., Krishnamurthy, R., De, V., Borkar, S., and Svensson, C., "Bitline leakage equalization for sub-100nm caches," in *Solid-State Circuits Conference, 2003. ESSCIRC'03. Proceedings of the 29th European*, pp. 401–404, Sept. 2003.

[4] Arden, W., Brillouet, M., Cogez, P., Graef, M., Huizing, B., and Mahnkopf, R., "More-than-Moore white paper." http://www.itrs.net/Links/2010ITRS/IRC-ITRS-MtM-v2%203.pdf.

[5] Brown, W., "The history of power transmission by radio waves," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 32, no. 9, pp. 1230–1242, 1984.

[6] Cha, J., Ahn, M., Cho, C., Lee, C., Kim, H., and Laskar, J., "Analysis and design techniques of cmos charge-pump-based radio-frequency antenna-switch controllers," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 56, no. 5, pp. 1053–1062, 2009.

[7] Chang, L., Fried, D., Hergenrother, J., Sleight, J., Dennard, R., Montoye, R., Sekaric, L., McNab, S., Topol, A., Adams, C., and others, "Stable SRAM cell design for the 32 nm node and beyond," in *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 128–129, Jun. 2005.

[8] Cook, B., Lanzisera, S., and Pister, K., "SoC issues for RF smart dust," *Proceedings of the IEEE*, vol. 94, pp. 1177–1196, June 2006.

[9] Cosemans, S., Dehaene, W., and Catthoor, F., "A 3.6 pj/access 480 mhz, 128 kb on-chip sram with 850 mhz boost mode in 90 nm cmos with tunable sense amplifiers," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 7, pp. 2065–2077, 2009.

[10] Eberly, W., Giesbrecht, M., and Villard, G., "On computing the determinant and Smith form of an integer matrix," in *Proceedings. 41st Annual Symposium on Foundations of Computer Science*, Nov. 2000.

[11] Enz, C. and Vittoz, E., *Charge-based MOS transistor modeling*. Chichester, England: Wiley, 2006.

[12] Erickson, R. and Maksimović, D., *Fundamentals of power electronics*. Springer Netherlands, 2001.

[13] Frantz, G., "Digital signal processor trends," *Micro, IEEE*, vol. 20, pp. 52–59, Nov./Dec. 2000.

[14] Gerald, J., Tavares, G., Piedade, M., Varela, E., and Ribeiro, R., "Rf-link for cortical neuroprosthesis," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, pp. 2739–2742, 2005.

[15] Ghovanloo, M. and Najafi, K., "Fully integrated wideband high-current rectifiers for inductively powered devices," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 11, pp. 1976–1984, 2004.

[16] Ghovanloo, M. and Najafi, K., "A wideband frequency-shift keying wireless link for inductively powered biomedical implants," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 51, no. 12, pp. 2374–2383, 2004.

[17] Gravati, M., Valle, M., Ferri, G., Guerrini, N., and Reyes, N., "A novel current-mode very low power analog CMOS four quadrant multiplier," in *Proceedings of the 31st European Solid-State Circuits Conference*, pp. 495–498, Sep. 2005.

[18] Harrison, R., Watkins, P., Kier, R., Lovejoy, R., Black, D., Greger, B., and Solzbacher, F., "A low-power integrated circuit for a wireless 100-electrode neural recording system," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 1, pp. 123–133, 2007.

[19] Hu, Y. and Sawan, M., "A fully integrated low-power bpsk demodulator for implantable medical devices," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, no. 12, pp. 2552–2562, 2005.

[20] Huang, Q. and Oberle, M., "A 0.5-mw passive telemetry ic for biomedical applications," *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 7, pp. 937–946, 1998.

[21] Kendir, G., Liu, W., Bashirullah, R., Wang, G., Humayun, M., and Weiland, J., "An efficient inductive power link design for retinal prosthesis," in *Circuits and Systems, 2004. ISCAS'04. Proceedings of the 2004 International Symposium on*, vol. 4, pp. IV–41, May 2004.

[22] Kinget, P., "Device mismatch and tradeoffs in the design of analog circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1212–1224, Jun. 2005.

[23] Lam, Y., Ki, W., and Tsui, C., "Integrated low-loss cmos active rectifier for wirelessly powered devices," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 53, no. 12, pp. 1378–1382, 2006.

[24] Lee, S., Yoo, J., Kim, H., and Yoo, H., "A dynamic real-time capacitor compensated inductive coupling transceiver for wearable body sensor network," in *VLSI Circuits, 2009 Symposium on*, pp. 42–43, Jun. 2009.

[25] Lee, S., Song, T., Park, J., Cho, C., An, S., Lim, K., and Laskar, J., "A cmos integrated analog pulse compressor for mimo radar applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, no. 4, pp. 747–756, 2010.

[26] Lim, K. and Laskar, J., "Emerging opportunities of RF IC/system for future cognitive radio wireless communications," in *Radio and Wireless Symposium, 2008 IEEE*, pp. 703–706, Jan. 2008.

[27] Lin, J., "Studies on microwaves in medicine and biology: From snails to humans," *Bioelectromagnetics*, vol. 25, no. 3, pp. 146–159, 2004.

[28] Liu, W., Vichienchom, K., Clements, M., DeMarco, S., Hughes, C., McGucken, E., Humayun, M., De Juan, E., Weiland, J., and Greenberg, R., "A neuro-stimulus chip with telemetry unit for retinal prosthetic device," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 10, pp. 1487–1497, 2000.

[29] Mandal, S. and Sarpeshkar, R., "A bidirectional wireless link for neural prostheses that minimizes implanted power consumption," in *Biomedical Circuits and Systems Conference, 2007. BIOCAS 2007. IEEE*, pp. 45–48.

[30] Mandal, S. and Sarpeshkar, R., "Low-power cmos rectifier design for rfid applications," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 54, no. 6, pp. 1177–1188, 2007.

[31] Neihart, N. and Harrison, R., "Micropower circuits for bidirectional wireless telemetry in neural recording applications," *Biomedical Engineering, IEEE Transactions on*, vol. 52, no. 11, pp. 1950–1959, 2005.

[32] Noguchi, H., Okumura, S., Iguchi, Y., Fujiwara, H., Morita, Y., Nii, K., Kawaguchi, H., and Yoshimoto, M., "Which is the best dual-port SRAM in 45-nm process technology? 8t, 10t single end, and 10t differential?," in *Integrated Circuit Design and Technology and Tutorial, 2008. ICICDT 2008. IEEE International Conference on*, pp. 55–58, Jun. 2008.

[33] Nowak, E. J., "Maintaining the benefits of cmos scaling when scaling bogs down," *IBM Journal of Research and Development*, vol. 46, pp. 169 –180, March 2002.

[34] O'Driscoll, S., Poon, A., and Meng, T., "A mm-sized implantable power receiver with adaptive link compensation," in *Solid-State Circuits Conference-Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, pp. 294–295, Feb. 2009.

[35] Park, J., Song, T., Hur, J., Lee, S., Choi, J., Kim, K., Lim, K., Lee, C., Kim, H., and Laskar, J., "A fully integrated uhf-band cmos receiver with multi-resolution spectrum sensing (mrss) functionality for ieee 802.22 cognitive radio applications," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 1, pp. 258–268, 2009.

[36] Peters, C., Kessling, O., Henrici, F., Ortmanns, M., and Manoli, Y., "Cmos integrated highly efficient full wave rectifier," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, pp. 2415–2418, May 2007.

[37] Pottie, G. and Kaiser, W., "Wireless integrated network sensors," *Communications of the ACM*, vol. 43, no. 5, pp. 51–58, 2000.

[38] Rabaey, J., Ammer, J., Karalar, T., Li, S., Otis, B., Sheets, M., and Tuan, T., "Picoradios for wireless sensor networks: the next challenge in ultra-low power design," in *Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International*, vol. 1, pp. 200–201, Feb. 2002.

[39] Shibata, N., Kiya, H., Kurita, S., Okamoto, H., Tan'no, M., and Douseki, T., "A 0.5-v 25-mhz 1-mw 256-kb mtcmos/soi sram for solar-power-operated portable personal digital equipment-sure write operation by using step-down negatively overdriven bitline scheme," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 3, pp. 728–742, 2006.

[40] Shin, J., Chung, I., Park, Y., and Min, H., "A new charge pump without degradation in threshold voltage due to body effect [memory applications]," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 8, pp. 1227–1230, 2000.

[41] Sodagar, A., Wise, K., and Najafi, K., "A fully integrated mixed-signal neural processor for implantable multichannel cortical recording," *Biomedical Engineering, IEEE Transactions on*, vol. 54, no. 6, pp. 1075–1088, 2007.

[42] Song, T., Kim, S., Lim, K., and Laskar, J., "Fully-gated ground 10t-sram bitcell in 45 nm soi technology," *Electronics letters*, vol. 46, no. 7, pp. 515–516, 2010.

[43] Umeda, T., Yoshida, H., Sekine, S., Fujita, Y., Suzuki, T., and Otaka, S., "A 950-mhz rectifier circuit for sensor network tags with 10-m distance," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 1, pp. 35–41, 2006.

[44] Von Arx, J. and Najafi, K., "On-chip coils with integrated cores for remote inductive powering of integrated microsystems," in *Solid State Sensors and Actuators, 1997. TRANSDUCERS'97 Chicago., 1997 International Conference on*, vol. 2, pp. 999–1002, Jun. 1997.

[45] Wang, G., Liu, W., Sivaprakasam, M., and Kendir, G., "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, no. 10, pp. 2109–2117, 2005.

[46] Wang, Y., Ahn, H., Bhattacharya, U., Chen, Z., Coan, T., Hamzaoglu, F., Hafez, W., Jan, C., Kolar, P., Kulkarni, S., and others, "A 1.1 ghz 12 μa/mb-leakage sram design in 65 nm ultra-low-power cmos technology with integrated leakage reduction for mobile applications," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 1, pp. 172–179, 2008.

[47] Winter, M. and Brodd, R., "What are batteries, fuel cells, and supercapacitors?," *Chemical reviews*, vol. 104, no. 10, pp. 4245–4270, 2004.

[48] Yoo, J., Lee, S., and Yoo, H., "A 1.12 pj/b inductive transceiver with a fault-tolerant network switch for multi-layer wearable body area network applications," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 11, pp. 2999–3010, 2009.

[49] Ziaie, B., Nardin, M., Coghlan, A., and Najafi, K., "A single-channel implantable microstimulator for functional neuromuscular stimulation," *Biomedical Engineering, IEEE Transactions on*, vol. 44, no. 10, pp. 909–920, 1997.

VITA

Stephen T. Kim received the B.S. degree from Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2007 and the M.S. degree in electrical and computer engineering from Georgia Institute of Technology, Atlanta, GA, where he is currently working towards the Ph.D. In 2010, he was an intern with Intersil in Atlanta, GA, where he worked as an IC designer to develop low-power CMOS signal integrity IC products. His research interests include low-power analog and mixed signal circuit design.